650V GaN Power Transistor (FET)

Features

* V_{DSS}=650V, I_D=9A
* Easy to use, compatible with standard gate drivers
* Excellent Q_g X $R_{DS(on)}$ figure of merit (FOM)
* Low Q_{rr}, No free-wheeling diode required
* Low Switching Loss
* Lead Free Available(RoHS Compliant)
* DFN-8X8-3L Packages

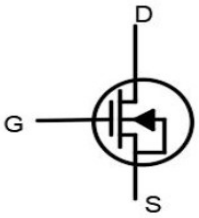
Applications

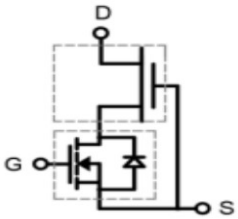
* High Efficiency Power Supplies
* High Efficiency USB PD Adapters
* Other Consumer Electronics

Product Summary		
V_{DSS}	650	V
$R_{DS(on)}$, Typ.	240	mΩ
Q_G, Typ.	21.5	nC
Q_{RR}, Typ.	39	nC

Pin Description and Schematic

DFN-8X8-3L





Cascode
Device Structure

Package Marking And Ordering Information

Device	Marking	Device Package	Quantity
SWGN9N65DN3L/TR	GN9N65DN3	DFN-8X8-3L	2500pcs, Tape&Reel

ABSOLUTE MAXIMUM RATINGS (T_j = 25'C UNLESS OTHERWISE NOTED)

Parameter		Symbol	SWGN9N65DN	Unit
Drain to Source Voltage (T_J=-55'C to 150'C)		V_{DSS}	650	V
Gate to Source Voltage		V_{GSS}	±20	V
Coutinuous Drain Current	T_C=25'C	I_D	9	A
	T_C=100'C		6	A
Pulsed Drain Current (pulse width:10us)	T_C=25'C	I_{DM}	31	A
	T_C=150'C		23	
Maximum Power Dissipation	T_C=25'C	P_D	38	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	'C
Soldering Peak Temperature		T_{CSOLD}	260	'C
Thermal Resistance, Junction-to-Case(Maximum)		R_{QJC}	3.3	'C/W
Thermal Resistance, Junction-to-Ambient(Maximum)[note2]		R_{QJA}	50	'C/W

Note 1. Device on one layer epoxy PCB for drain connection(vertical and without air stream cooling with 6cm2 copper area and 70um thickness)

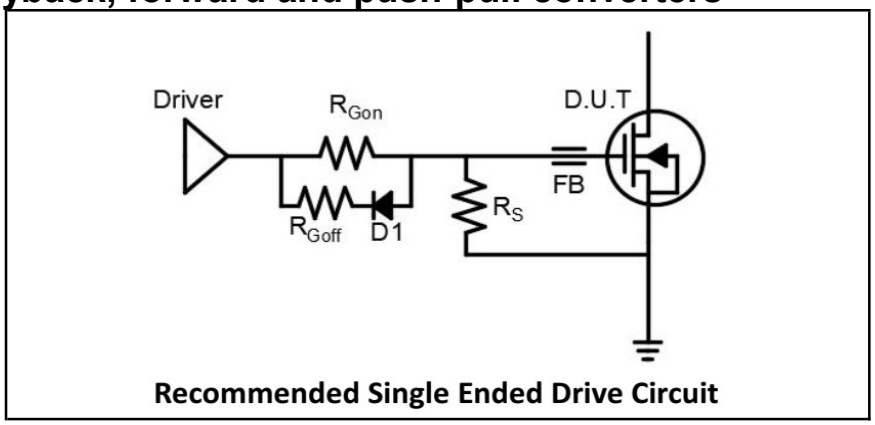
Electrical Characteristics (TA = 25'C unless otherwise noted)

Parameter	Symbol	Test Conditions	SWGN9N65DN			Unit
			Min	Typ	Max	
Forward Device Characteristics						
Drain -Source Breakdown Voltage	$V_{DSS-MAX}$	V_{GS}=0V,	650	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=700V, V_{GS}=0V, T_J=25'C	-	8	20	uA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=700V, V_{GS}=0V, T_J=100'C	-	50	-	
Gate-Body Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}= ±20V	-	-	±150	nA
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D= 500uA	1.2	1.6	2.0	V
Drain-Source-On-Resistance note4	$R_{DS(on)}$	V_{GS}=8V, I_{DS}=4A, Tj=25'C	190	240	290	mΩ
		V_{GS}=8V, I_{DS}=4A, Tj=150'C	-	500	-	mΩ
Dynamic Characteristics						
Input Capacitance	C_{ISS}	V_{DS}= 650V, V_{GS}= 0V F=1MHz	-	500	-	pF
Output Capacitance	C_{OSS}		-	18	-	
Reverse Transfer Capacitance	C_{RSS}		-	2	-	
Output Capacitance(er)	$C_{O(er)}$	V_{DS}= 0-650V, V_{GS}= 0V	-	25	-	pF
Output Capacitance(tr)	$C_{O(tr)}$		-	45	-	
Turn-On Delay Time	$t_{d(ON)}$	V_{DS}=400V,I_{DS}=3A, V_{GS}=0-12V, R_G=30Ω	-	20	-	ns
Rise Time	t_r		-	7	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	80	-	ns
Fall Time	t_f		-	6	-	ns
Gate Charge Characteristics						
Total Gate Charge	Q_g	V_{DS}= 400V, V_{GS}= 0-12V I_{DS}=5.5A	-	21.5	-	nC
Gate-Source Charge	Q_{gs}		-	3.0	-	
Gate-Drain Charge	Q_{gd}		-	3.5	-	
Reverse Diode Characteristics						
Diodes Forward Voltage note4	V_{SD}	V_{GS}=0V, I_{DS}=2A, T_J=25'C	-	1.2	-	V
		V_{GS}=0V, I_{DS}=5A, T_J=25'C	-	1.7	-	V
		V_{GS}=0V, I_{DS}=5A, T_J=150'C	-	2.0	-	V
Reverse Recovery Time	t_{rr}	I_S=3A, V_{GS}=0V, V_{DD}=400V, di/dt=1000A/us(Note3)	-	12	-	nS
Reverse Recovery Charge	Q_{rr}		-	39	-	uC

Note 4. Dynamic on-resistance;

Circuit Implementation

Mostly used in flyback, forward and push-pull converters

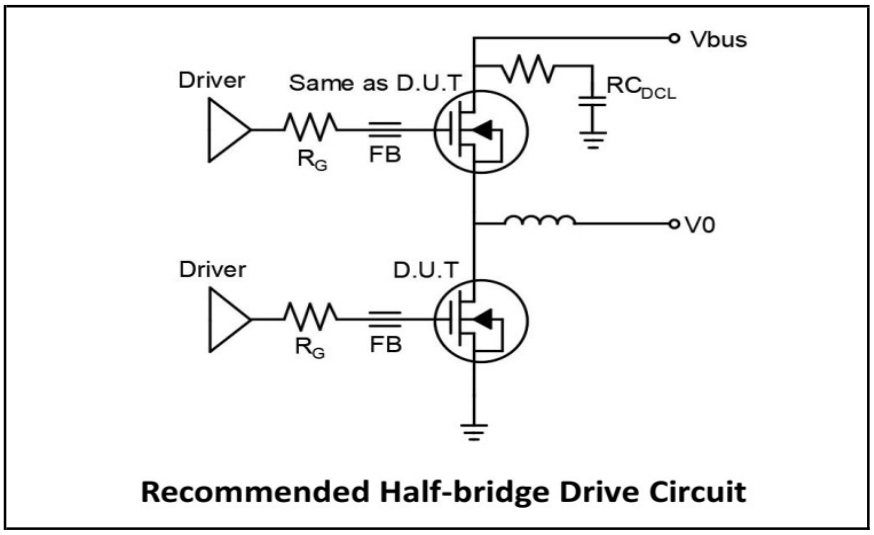


Recommended Single Ended Drive Circuit

Recommended gate drive: (0V, 12V) with Rgon=300 - 500Ω, Rgoff=10Ω

Gate Ferrite Bead (FB)	Gate Resistance (R_{Gon})	Gate Resistance (R_{Goff})	Gate Source Resistance (R_S)	Gate Diode (D1)
300-600Ω@100MHz	300-500Ω	10Ω	10KΩ	1N4148

Mostly used in half bridge and full bridge topology



Recommended Half-bridge Drive Circuit

Recommended gate drive: (0V, 12V) with R_G=30 - 70Ω

Gate Ferrite Bead (FB)	Gate Resistance (R_G)	DC Link RC Snubber (RC_{DCL})
300Ω@100MHz	30 - 70Ω	4nF + 2Ω

Notes:

a. RC_{DCL} should be placed as close as possible to the srain pin.

b. The layout and wiring of the drive circuit should be as short as possible.

Typical Characteristics (TJ = 25'C unless otherwise noted)

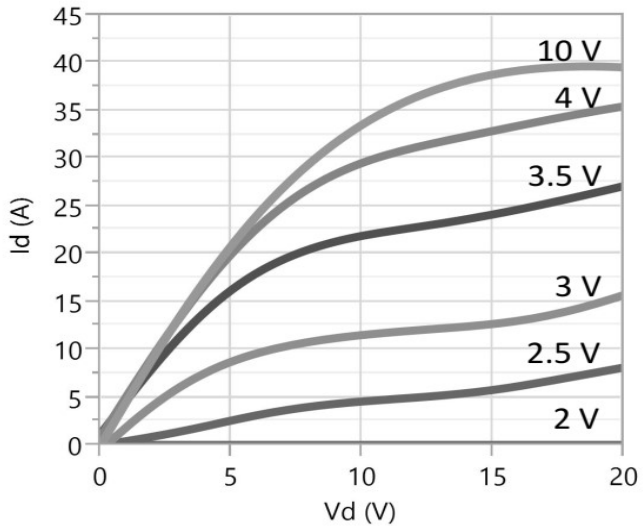


Figure 1: Typical Output Characteristics

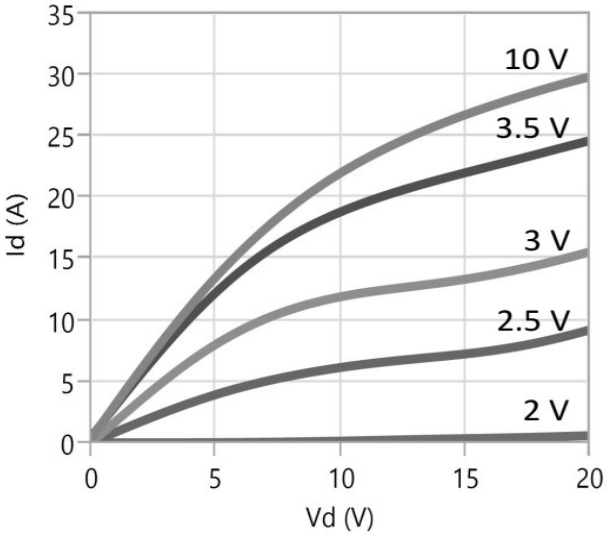


Figure 2: Typical Output Characteristics TJ=150'C

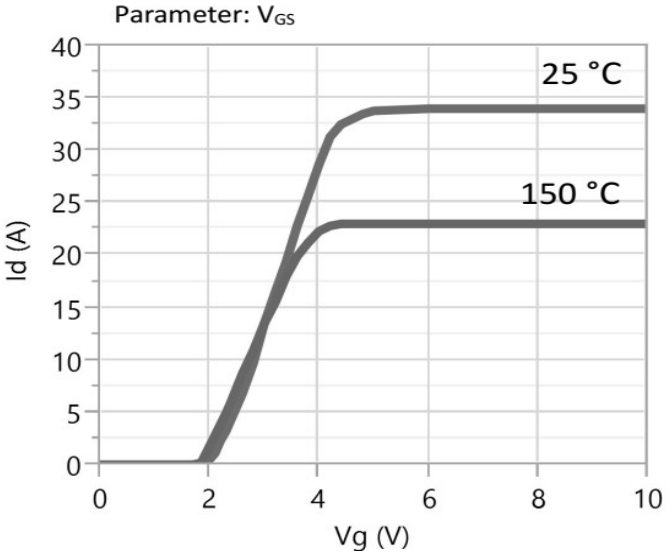


Figure 3: Typical Transfer Characteristics

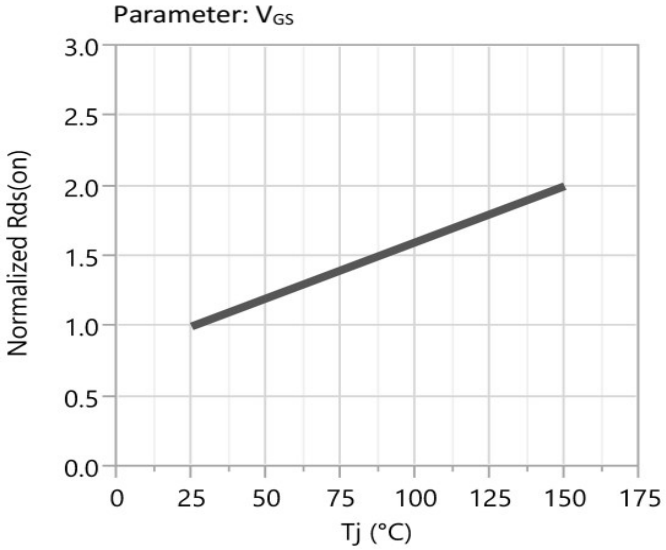


Figure 4: Normalized On-resistance

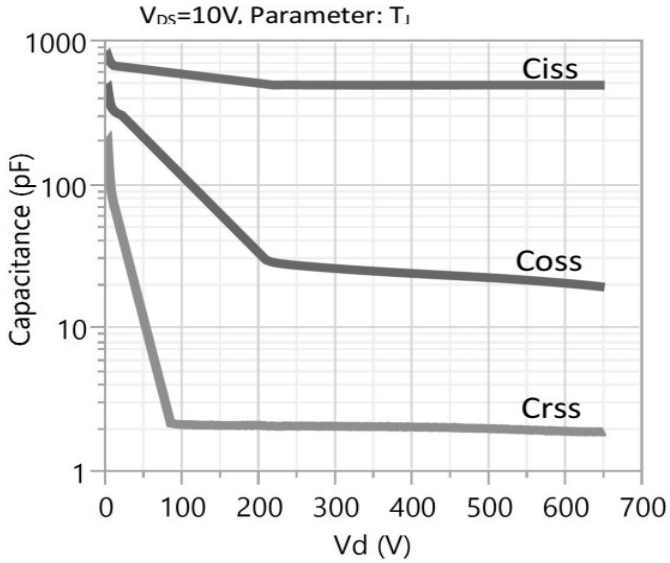


Figure 5: Typical Capacitance(VGS=0V, f=1MHz)

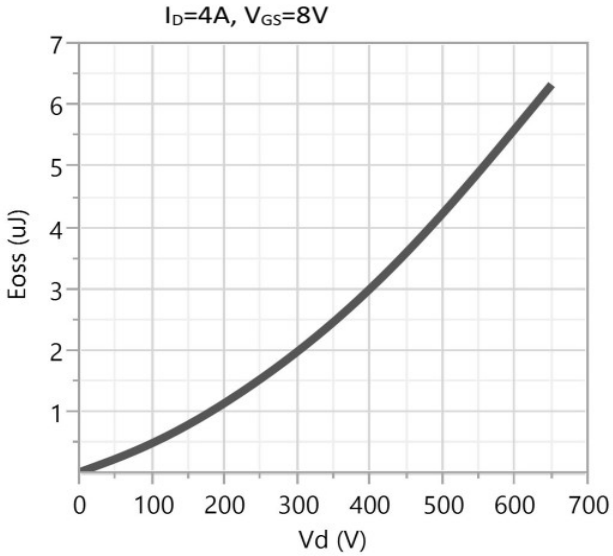


Figure 6: Typical Coss Stored Energy

Typical Characteristics (TJ = 25'C unless otherwise noted)(Con.)

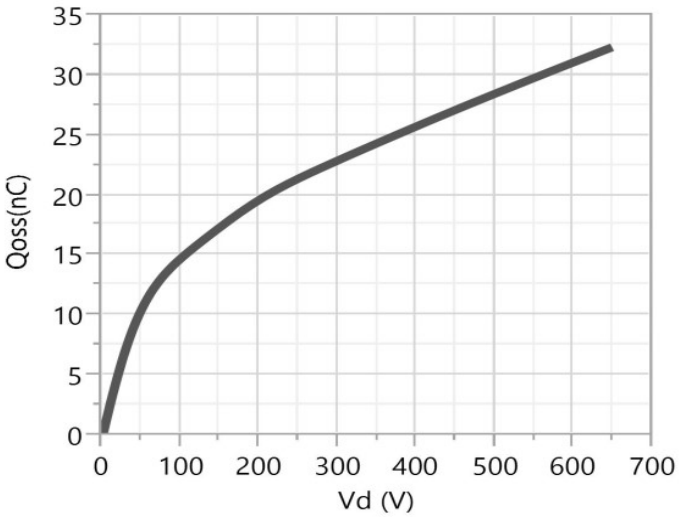


Figure 7: Typical Qoss

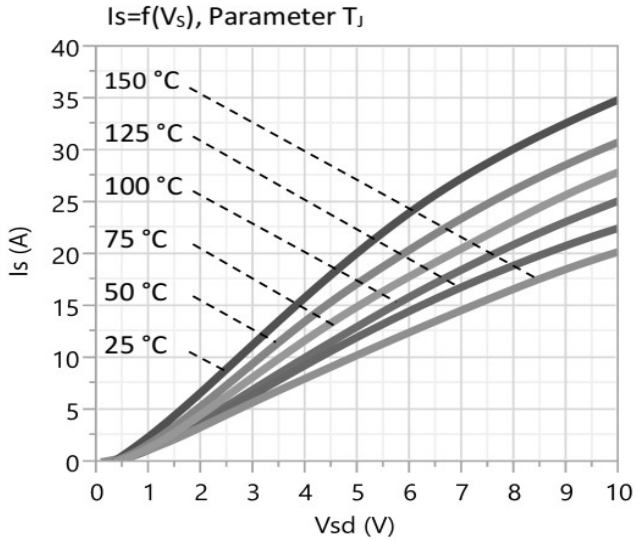


Figure 8: Forward Characteristic of Rev. Diode

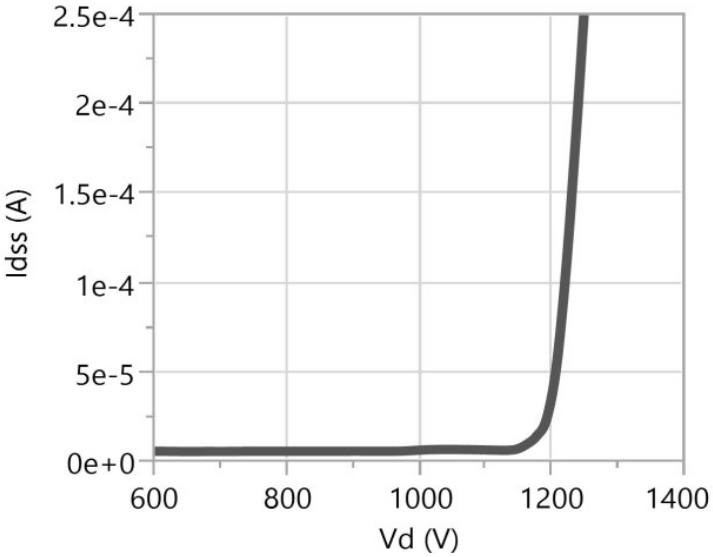


Figure 9: Drain-Source Breakdown Voltage

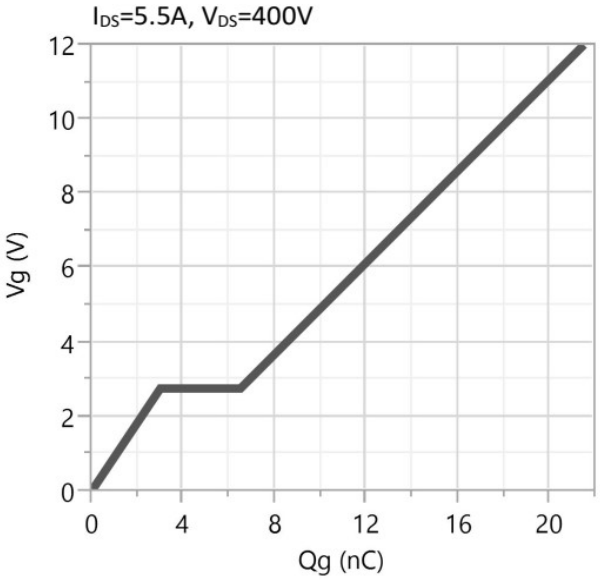


Figure 10: Typical Gate Charge

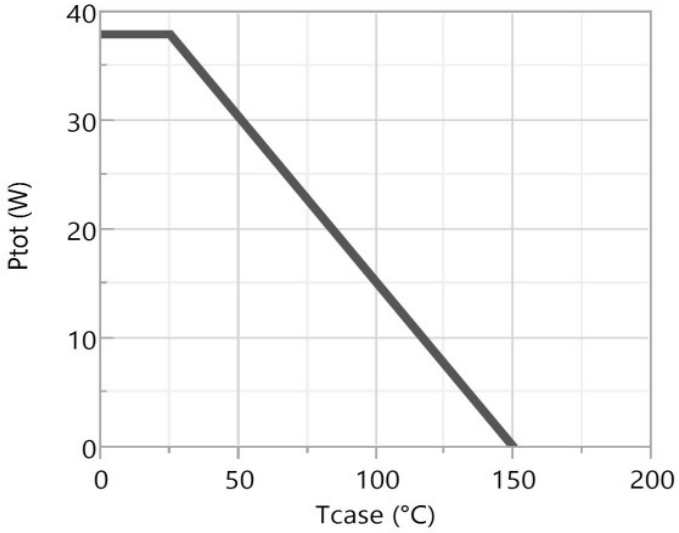


Figure 11: Power Dissipation

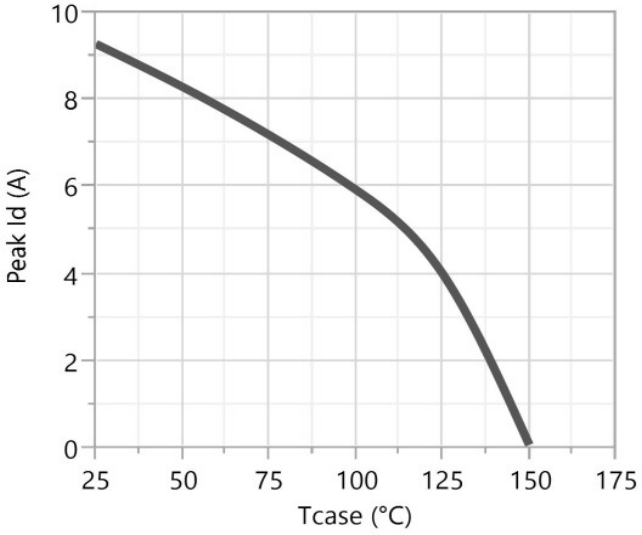


Figure 12: Current Derating

Typical Characteristics (TJ = 25'C unless otherwise noted)(Con.)

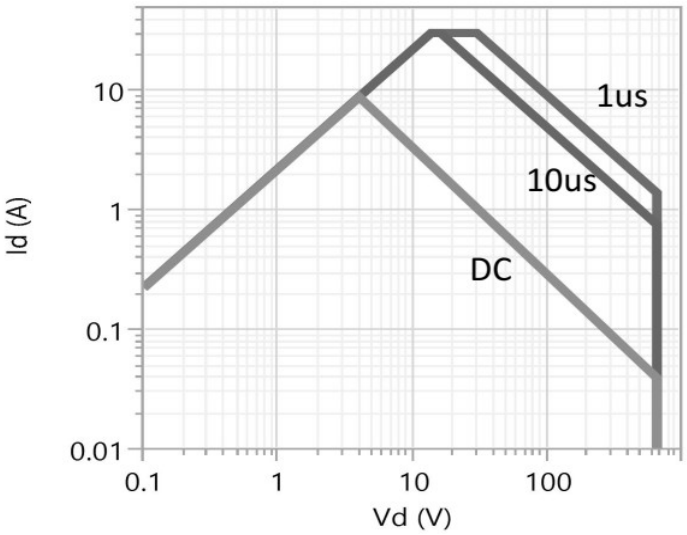


Figure 13: Safe Operating Area Tc=25'C

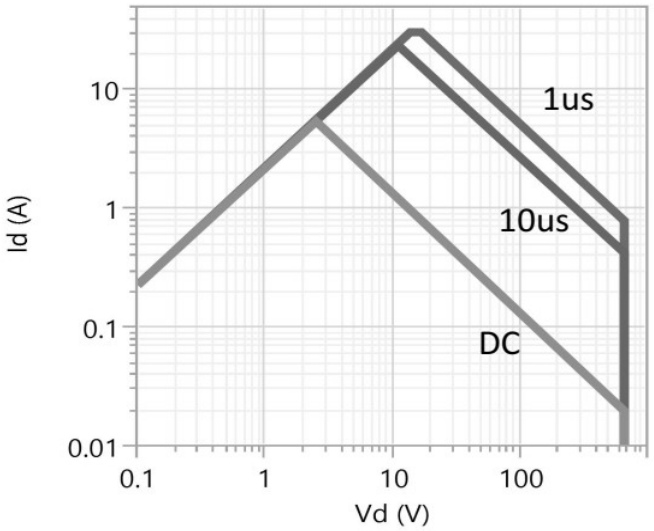


Figure 14: Safe Operating Area Tc=80'C

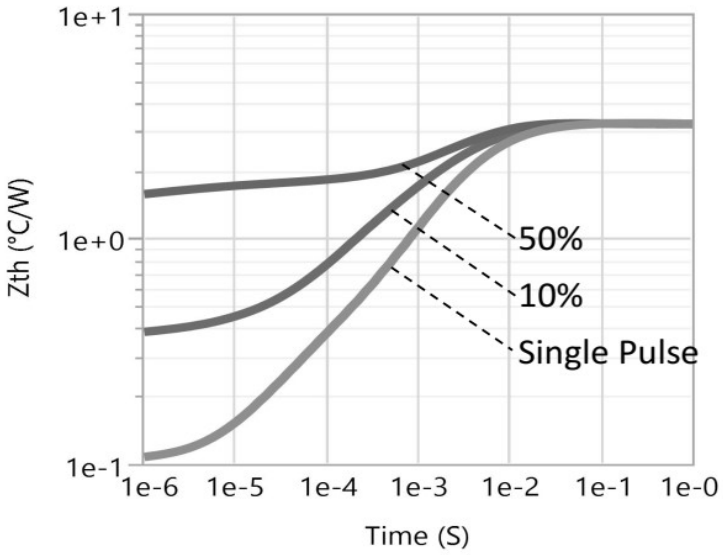
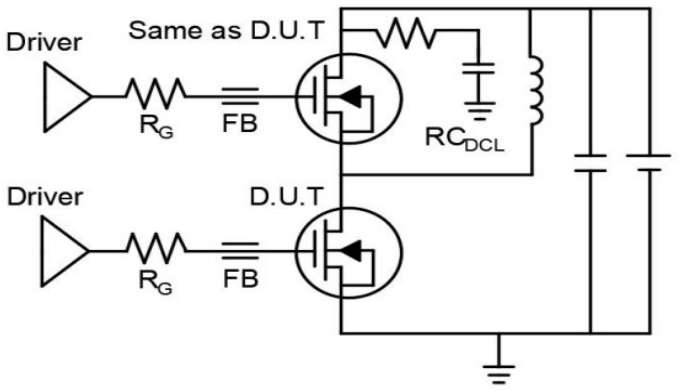
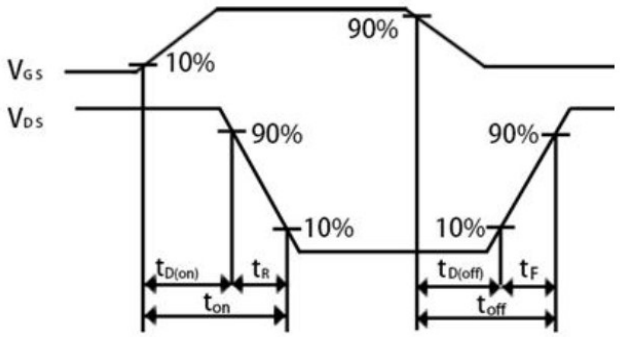


Figure 15: Transient Thermal Resistance

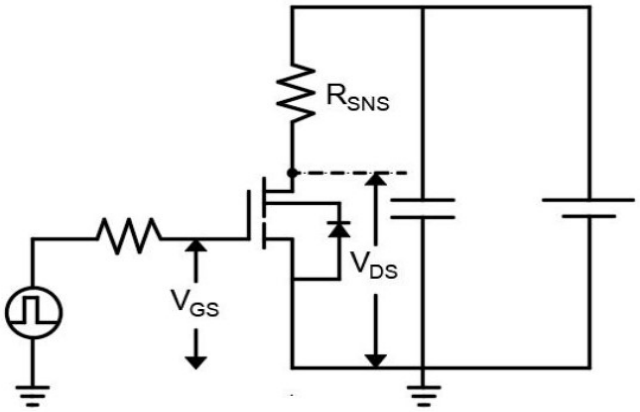
Test Circuit and Waveforms

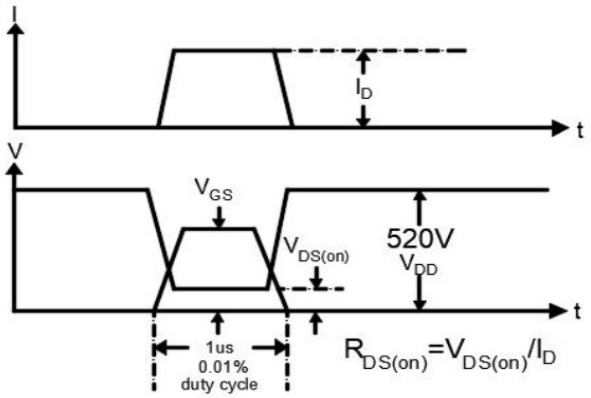
Switching Time Test Circuit and Waveform



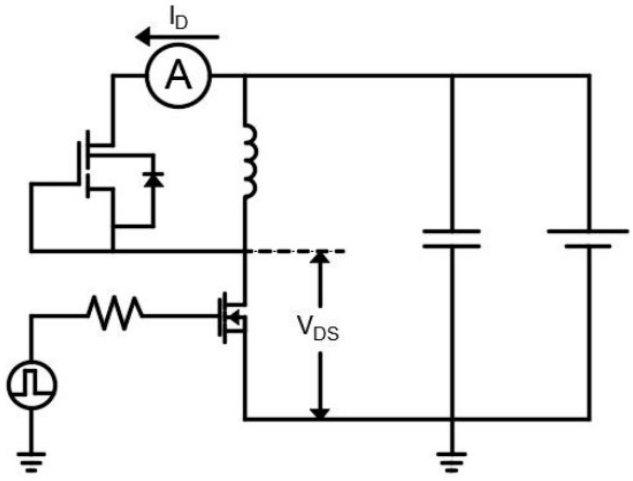


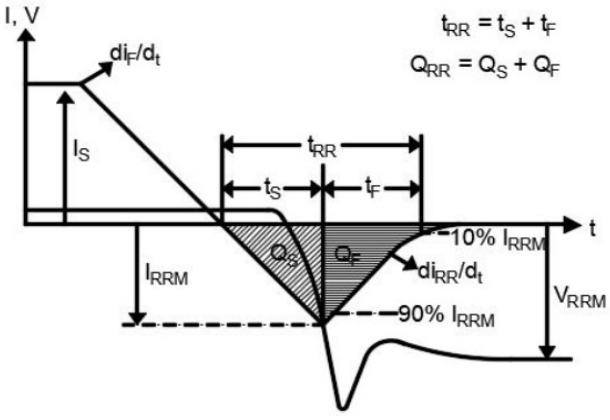
Dynamic $R_{DS(on)}$ Test Circuit and Waveform





Diode Characteristic Test Circuits and Waveform





Design Guidelines

Fast switching GaN device can reduce power conversion losses, and thus enable high frequency operations. Certain PCB design rules and instructions, however, need to be followed to take full advantages of fast switching GaN devices.

Before evaluating Star-wing's GaN devices, please refer to the table below which provides some practical rules that should be followed during the evaluation.

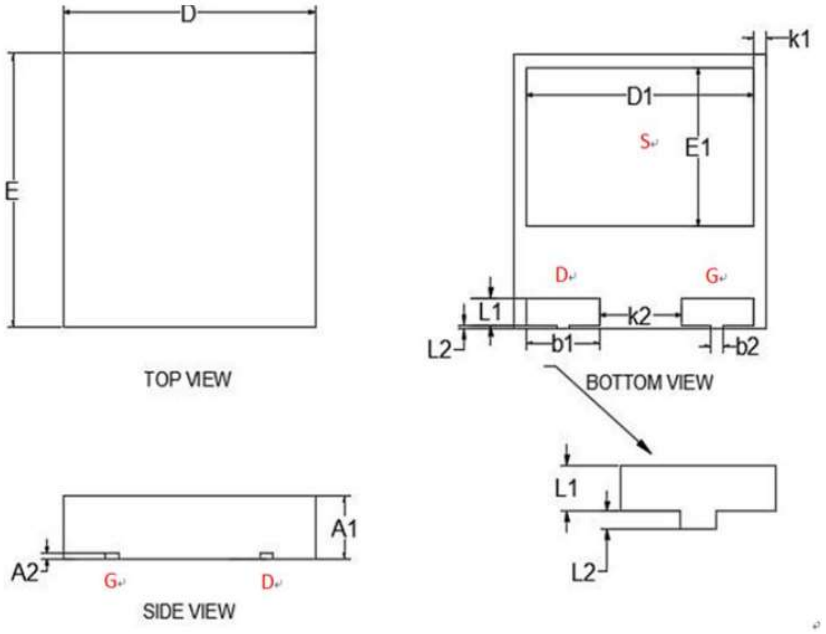
When Evaluating Star-wing's GaN Devices:

DO	DO NOT
Make sure the traces are as short as possible for both drive and power loops to minimize parasitic inductance	Using Star-wing devices in GDS board layouts
Use the test tool with the shortest inductive loop, and make sure test points should be placed close enough	Use differential mode probe or probe ground clip with long wires
Minimize the lead length of DFN-8X8-3L packages when installing them to PCB	Use long traces in drive circuit, or long lead length of the devices

Packaging Information

PKG: DFN-8X8-3L Package

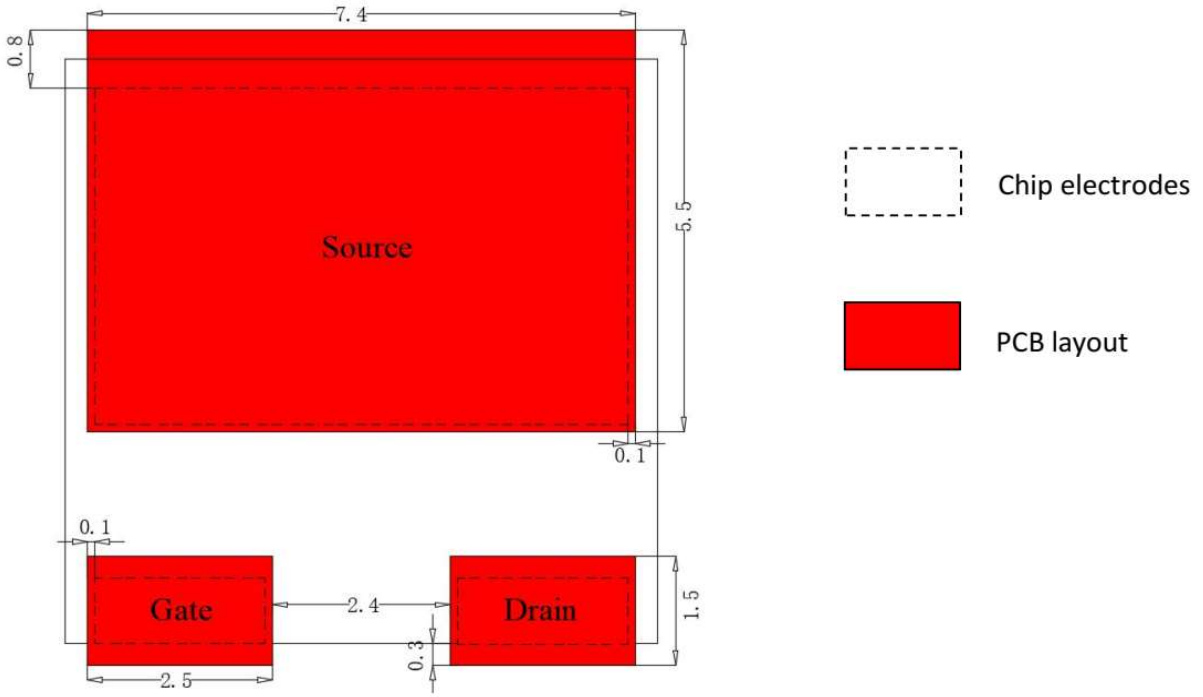
unit : mm



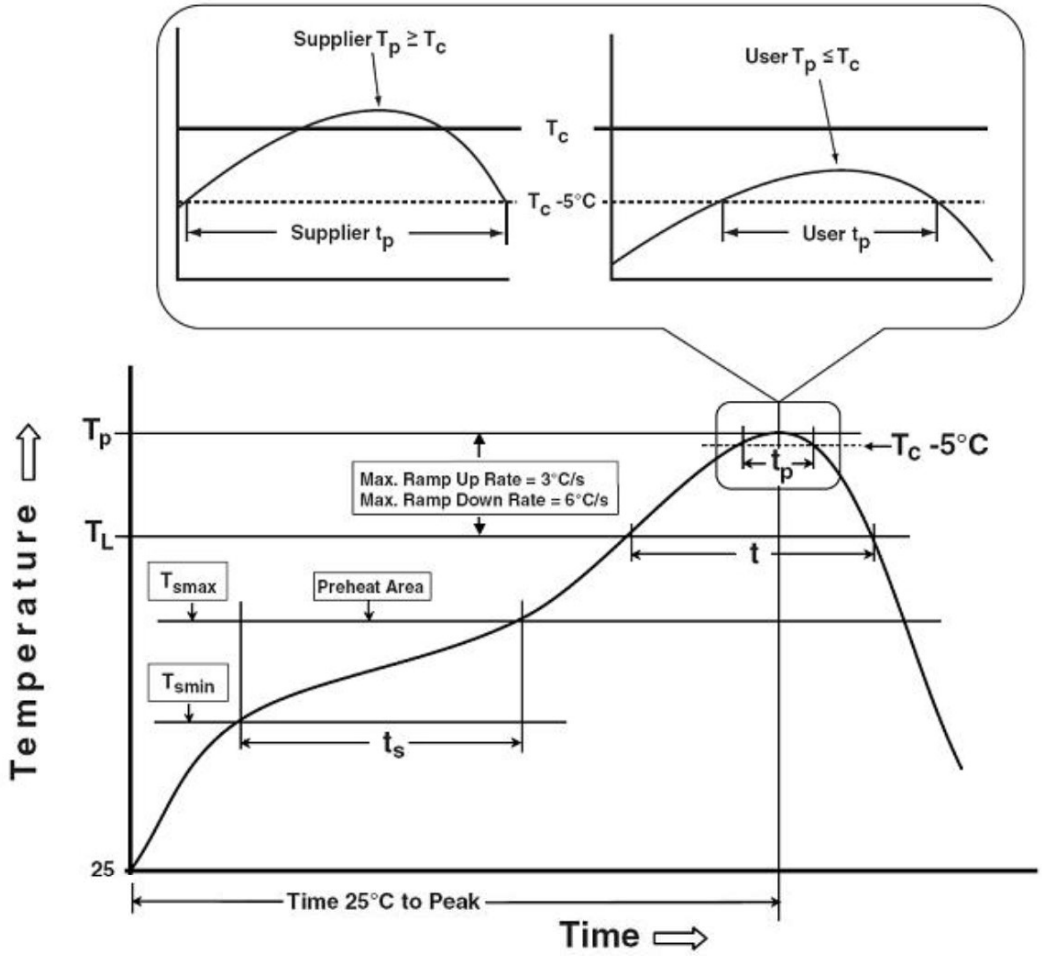
Symbol	Dimensions in Millimeters		
	MIN	NOM	MAX
A1	1.750	1.850	1.950
A2	0.185	0.203	0.230
D	7.000	8.000	9.000
E	7.950	8.000	8.050
D1	7.050	7.200	7.350
E1	4.450	4.600	4.750
K1	0.375	0.400	0.425
K2	2.575	2.600	2.625
b1	2.250	2.300	2.350
b2	0.375	0.400	0.425
L1	0.700	0.800	0.900
L2	0.075	0.100	0.125

Recommended PCB Layout

Dimensions are shown in millimeters



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (Tsmin to Tsmax) (t_s)	100 ℃ 150 ℃ 60-120 seconds	150 ℃ 200 ℃ 60-120 seconds
Average ramp-up rate ($T_{smax}$to T_P)	3 ℃/second max.	3℃/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 ℃ 60-150 seconds	217 ℃ 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	SeeClassification Tempin table 2
Time (t_P)** within 5℃ of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate ($T_p$to T_{smax})	6 ℃/second max.	6 ℃/second max.
Time 25℃ to peak temperature	6 minutes max.	8 minutes max.
*Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1.SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm³ <350	Volume mm³ ⩾350
＜2.5 mm	235 ℃	220 ℃
≥2.5 mm	220 ℃	220 ℃

Table 2.Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ ⩾2000
<1.6 mm	260 ℃	260 ℃	260 ℃
1.6 mm – 2.5 mm	260 ℃	250 ℃	245 ℃
⩾2.5 mm	250 ℃	245 ℃	245 ℃

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
PRECON	JESD-22, A113	30°C/60%/192Hrs
HTRB	JESD-22, A108	168/500/1000 Hrs, Bias @ 150°C
HTGB	JESD-22, A108	168 /500/1000Hrs, V_{gs}100% @ 150°C
PCT	JESD-22, A102	96 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -55°C~150°C