3.6MHz, Low Noise Rail-to-Rail I/O CMOS Operational Amplifier

Features

* High Gain Bandwidth : 3.6MHz
* Slew Rate: 1.8V/μs
* Input Offset Voltage: ±3mV(Max)
* Low Noise: 13nV/ √ Hz at 10KHz
* Rail-to-Rail Input and Output
* Supply Voltage Range: 2.5V to 5.5V
* Input Voltage Range: -0.1V to 5.6V with V_S = 5.5V
* Low Power
* Operating Temperature: -40'C to +125'C

Applications

* Sensors
* Photodiode Amplification
* Active Filters
* Test Equipment
* Driving A/D Converters

General Description [note a]

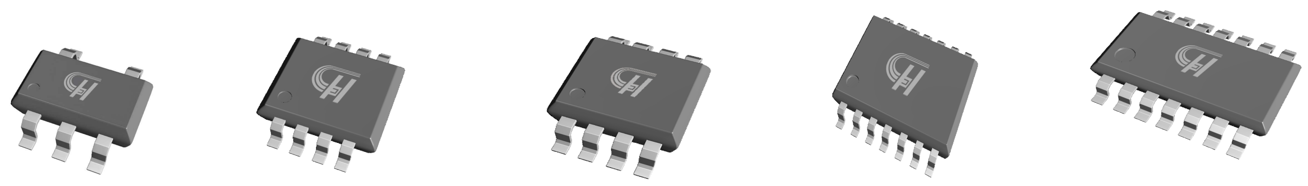
The HCR521(single)/HCR522(dual)/HCR524(quad) families of products offer low voltage operation and rail-to-rail input and output, as well as excellent speed/power consumption ratio, providing an excellent bandwidth (3.6MHz) and slew rate of 1.8V/μs. The op-amps are unity gain stable and feature an ultra-low input bias current.

The devices are ideal for sensor interfaces, active filters and portable applications. The HCR521/HCR522/HCR524 families of operational amplifiers are specified at the full temperature range of -40°C to +125°C under single or dual power supplies of 2.5V to 5.5V.

The HCR521 is available in Green SOT-23-5 packages.

The HCR522 is available in Green SOIC-8 and MSOP8 packages.

The HCR524 is available in Green SOIC-14 and TSSOP14 packages. They are specified over the extended industrial temperature range from -40 ℃ to +125℃.



SOT23-5 MSOP8 SOIC-8 TSSOP-14 SOIC-14

Figure 1. Package Type of HCR521/HCR522/HCR524

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Pin Configuration

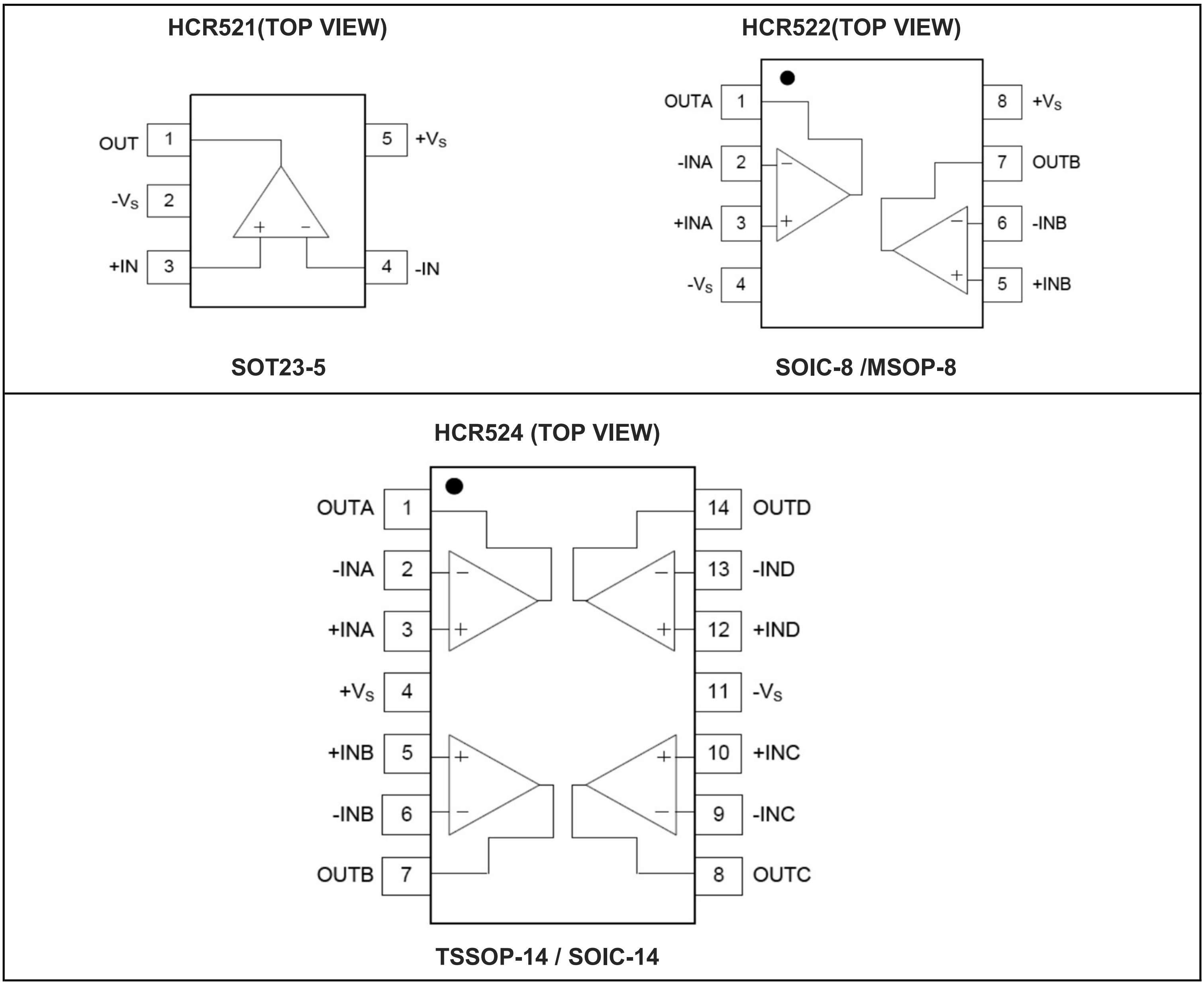

Figure 2. Pin Configuration of HCR521/HCR522/HCR524(Top View)

Pin Function Table

Name	Function
+IN, +INA, +INB, +INC, +IND	Non-inverting Inputs
-IN, -INA, -INB, -INC, -IND	Inverting Inputs
+Vs	Positive Power Supply
-Vs	Negative Power Supply
OUT, OUTA, OUTB, OUTC, OUTD	Outputs

Ordering Information

Type: HCR521 / HCR522 / HCR524 — Circuit Type

Package:
M5:SOT23-5
SM8:MSOP-8
M8: SOIC-8(SOP8)
M14: SOIC-14
TSP14: TSSOP-14

TR : Tape and Reel

Ordering Code

Part Number	Channel	Marking [1]	Op Temp('C)	MSL [2]	Package	Package Qty
HCR521/M5TR	1	521	-40'C to +125'C	MSL3	SOT23-5	3000pcs/TR
HCR522/SM8TR	2	HCR522xx	-40'C to +125'C	MSL3	MSOP-8	4000pcs/TR
HCR522/M8TR	2	HCR522xx	-40'C to +125'C	MSL3	SOIC-8 (SOP-8)	4000pcs/TR
HCR524/M14TR	4	HCR524xx	-40'C to +125'C	MSL3	SOIC-14 (SOP-14)	2500pcs/TR
HCR524/TSP14TR	4	HCR724xx	-40'C to +125'C	MSL3	TSSOP-14	4000pcs/TR

note 1: There may be additional marking, which relates to the lot trace code information(data code and vendor code)， the logo or the environmental category on the device.

2: HCRSEMI classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with HCRSEMI if your end application is quite critical to the preconditioning setting or if you have special requirement.

Absolute Maximum Ratings

Over operating free-air temperature range(unless otherwise noted) (3)

Parameter		Symbol	Value	Unit
Supply Voltage, +Vs to -Vs		V+	7.0	V
Signal Input Voltage		VIN	(V-)-0.5 to (V+)+0.5	V
Signal Output Voltage		Vout	(V-)-0.5 to (V+)+0.5	V
Signal Input Current		IIN	-10 to +10	mA
Signal Output Current		IO	-100 to +100	mA
Output Short-Circuit (4)		-	Continuous	
Thermal Resistance (5) @TA=+25'C	SOT23-5	θJA	230	'C/W
	SOIC-8	θJA	110	'C/W
	MSOP-8	θJA	170	'C/W
	SOIC-14	θJA	90	'C/W
	TSSOP-14	θJA	105	'C/W
Storage Temperature Range		TSTG	-65 to 150	'C
Operating Temperature Range		TOPR	-40 to +125	'C
Junction Temperature (6)		TJ	150	'C
Lead Temperature (Soldering, 10s)		TLEAD	260	'C
Human Body Model ESD Protection		ESD HBM	4	KV
Machine Model ESD Protection		ESD MM	400	V

note 3. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

4. Short-circuit to ground, one amplifier per package.
5. The package thermal impedance is calculated in accordance with JESD-51.
6. The maximum power dissipation is a function of TJ(MAX), RθJA, and TA. The maximum allowable power dissipation at any ambient temperature is PD = (T J(MAX) - TA) / RθJA. All numbers apply for packages soldered directly onto a PCB.

Recommended Operating Conditions

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage, +Vs to -Vs	Signal-supply	VIN	2.5	5.5	V
	Dual-supply		±1.25	±2.75	V
Operating Temperature Range		Ta	-40	+125	'C

Electrical Characteristics

(TA=25 `C, At Vs=+5V, RL=10KΩ VCM=Vs/2 .Unless Otherwise Specified.)

Parameter	Symbol	Conditions	Min	Type	Max	Unit
Input Characteristics						
Input Offset Voltage	VOS	VCM =Vs /2	-3.0	±0.8	3.0	mV
Input Bias Current:	IB		-	±1	±10	pA
Input Offset Current:	IOS		-	±1	±10	pA
Input Common Mode Voltage Range	VCM	Vs=5.5V	-0.1	-	+5.6	V
Common Mode Rejection Ratio	CMRR	Vs=5.5V, VCM=-0.1V to 4V	76	87	-	dB
		Vs=5.5V, VCM=-0.1V to 5.6V	62	71	-	
Open-Loop Voltage Gain	AOL	RL=2KΩ, Vout=+0.15V to 4.85V	100	107	-	dB
		RL=10KΩ, Vout=+0.05V to 4.95V	100	110	-	dB
Input Offset Voltage Drift	ΔVOS/ΔT		-	±2.0	-	uV/'C
Output Characteristics						
Output Voltage Swing from Rail	-	RL=2KΩ	-	31	-	mV
		RL=10KΩ	-	7	-	mV
Output Short-Circuit Current	IOUT		-	±80	-	mA
Power Supply						
Operating Voltage Range	Vs		2.5	-	5.5	V
Power Supply Rejection Ratio	PSRR	Vs=2.5V to 5.5V, VCM =(-Vs)+0.5V	76	86	-	dB
Quiescent Current per Amplifier	IQ		-	260	350	uA
Dynamic Performance						
Gain Bandwidth Product	GBP		-	3.6	-	MHz
Phase Margin	Øo	-	-	65	-	°
Slew Rate	SR	G=+1.2V Output Step	-	1.8	-	V/uS
Settling Time to 0.1%	ts	G=+1.2V Output Step	-	0.5	-	uS
Overload Recovery Time		VINxG>=Vs	-	0.7	-	uS
Noise Performance						
Input Voltage Noise Density	en	f=1KHz	-	15	-	nV/ √Hz
		f=10KHz	-	13	-	nV/ √Hz

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Typical Performance Characteristics.

(TA=25 `C, Vs=+5V, and RL=10KΩ connected to Vs/2, VOUT=Vs/2,Unless Otherwise Noted.)

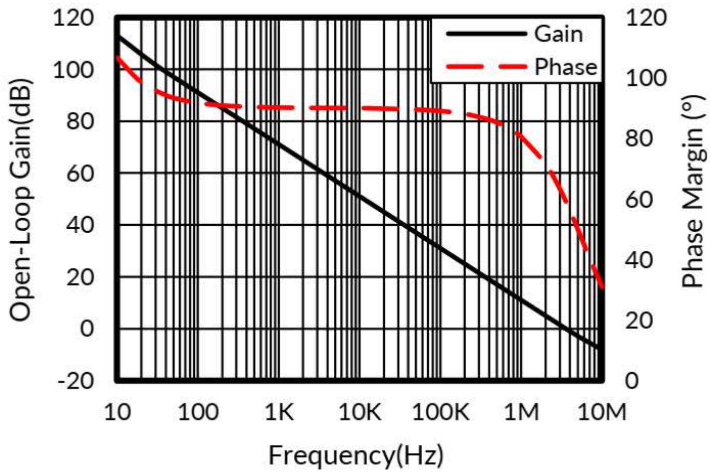

Figure 3. Open-Loop Gain and Phase vs Frequency

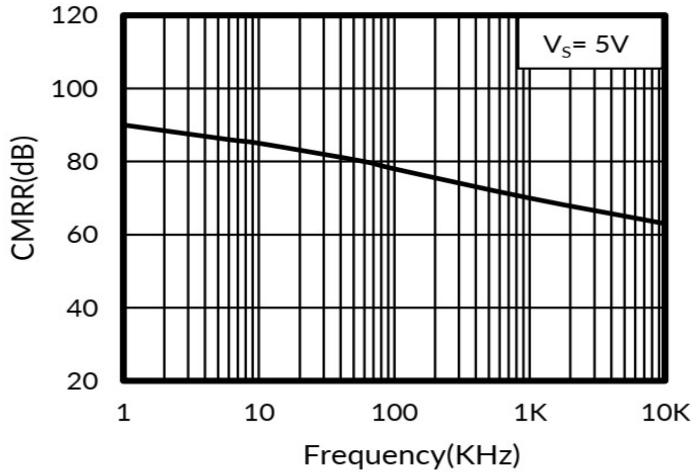

Figure 4. Common-Mode Rejection Ratio vs Frequency

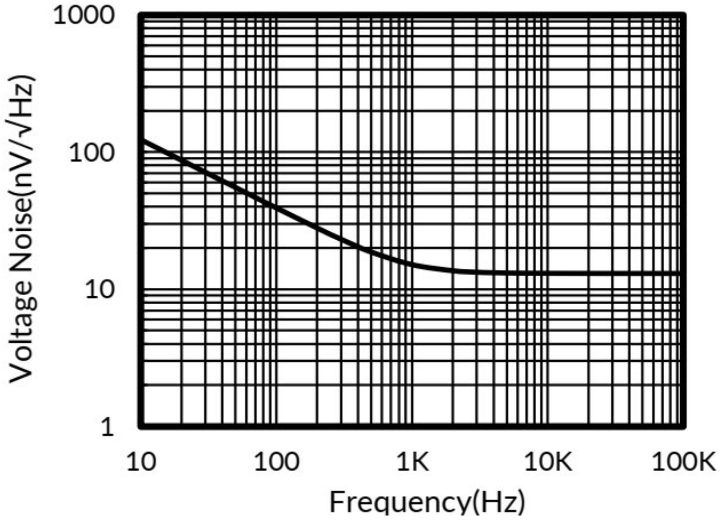

Figure 5. Input Voltage Noise Spectral Density vs Frequency

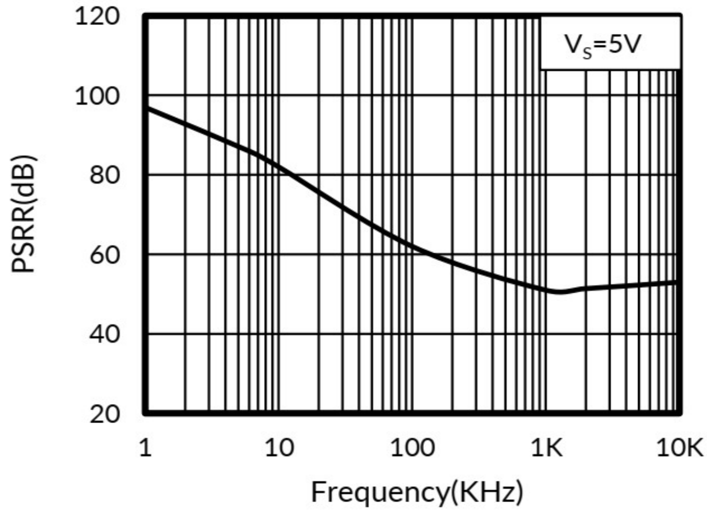

Figure 6. Power-Supply Rejection Ratio vs Frequency

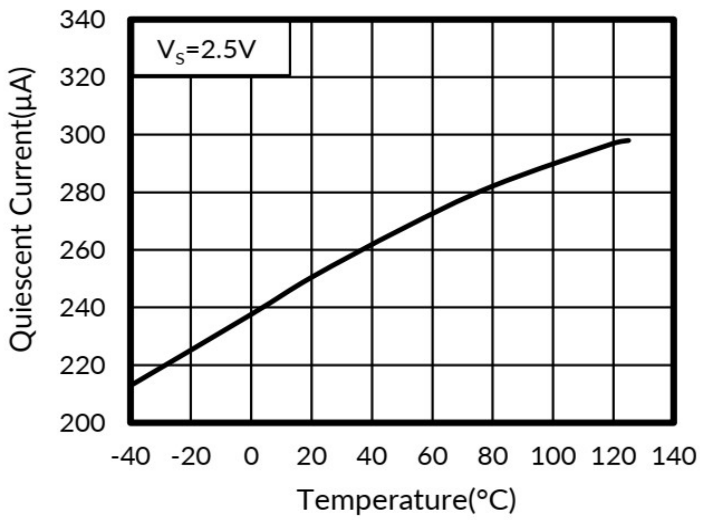

Figure 7. Quiescent Current vs Temperature

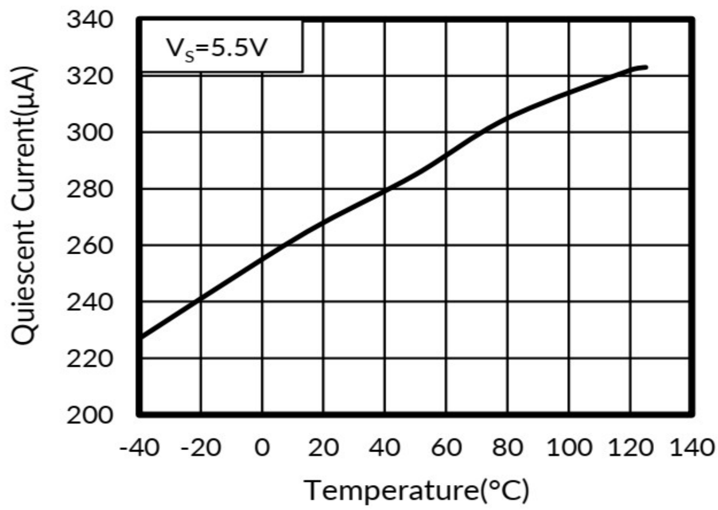

Figure 8. Quiescent Current vs Temperature

Typical Performance Characteristics(con.)

(TA=25 `C, Vs=+5V, and RL=10KΩ connected to Vs/2, VOUT=Vs/2,Unless Otherwise Noted.)

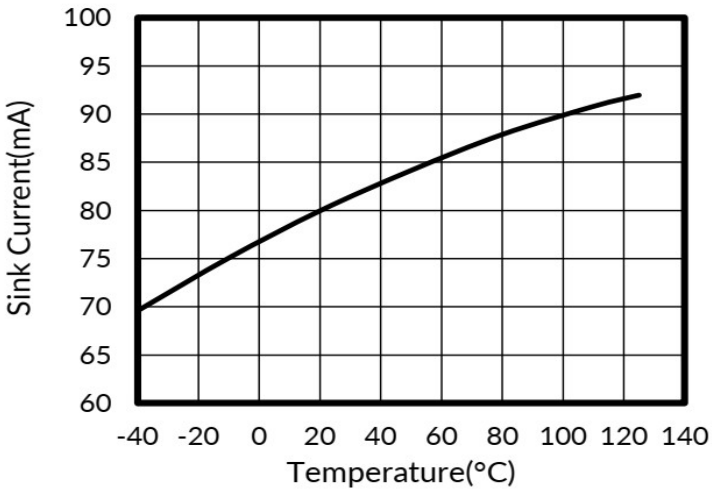

Figure 9. Sink Current vs Temperature

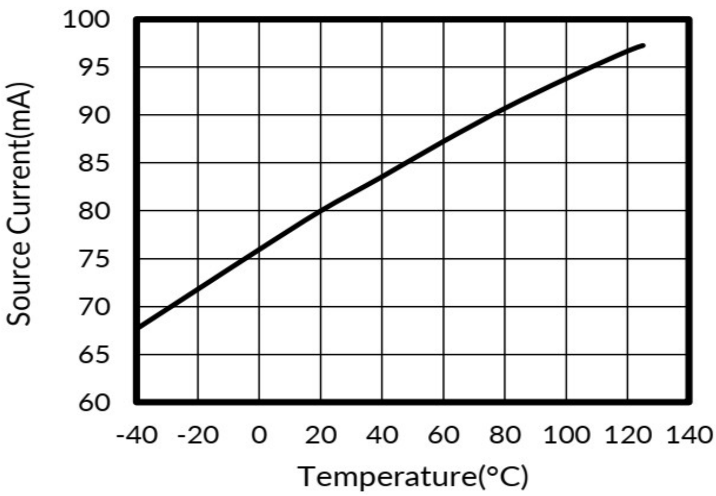

Figure 10. Source Current vs Temperature

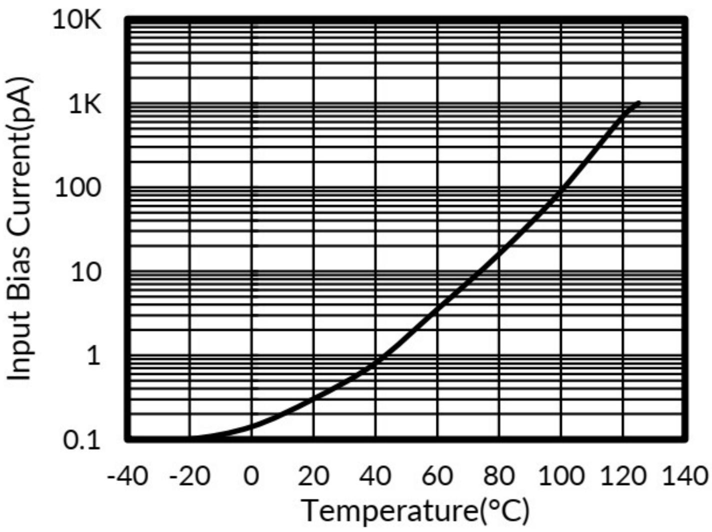

Figure 11. Input Bias Current vs Temperature

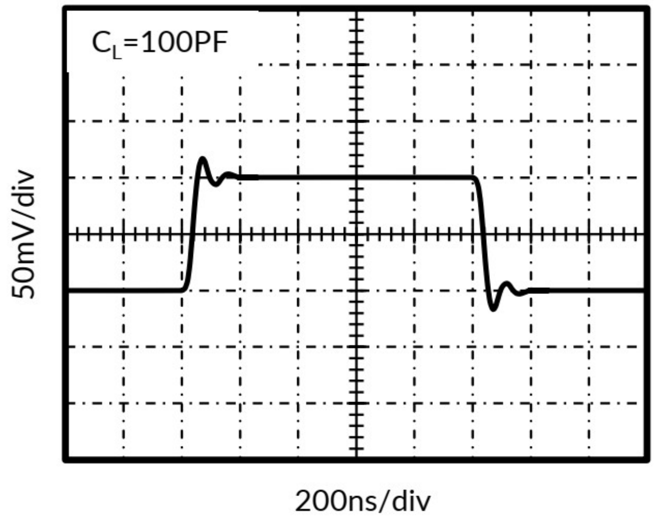

Figure 12. small-Signal Step Response

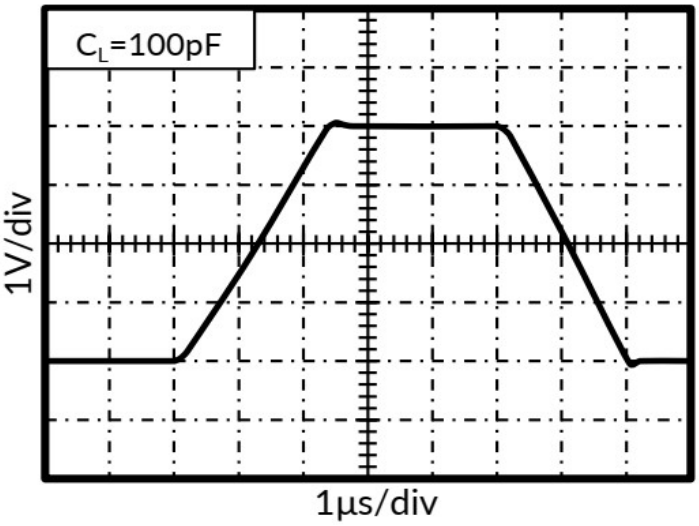

Figure 13. Large-Signal Step Response

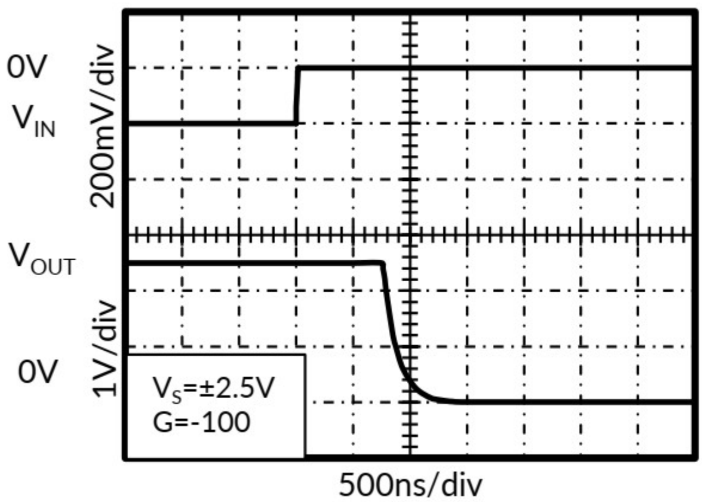

Figure 14. Positive Overload Recovery

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Typical Performance Characteristics(con.)

(TA=25 `C, Vs=+5V, and RL=10KΩ connected to Vs/2, VOUT=Vs/2,Unless Otherwise Noted.)

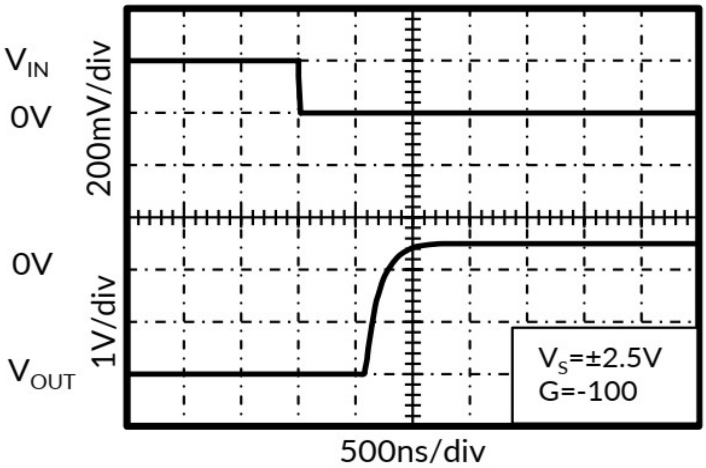


Figure 15. Negative Overload Recovery

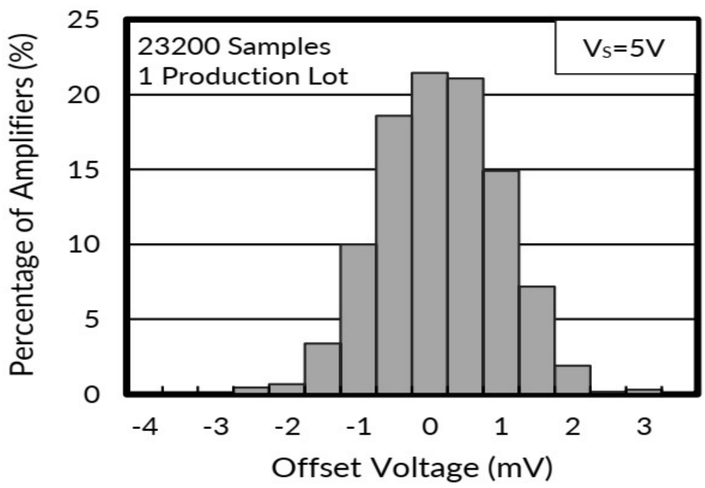


Figure 16. Offset Voltage Production Distribution

Detailed Description

Overview

The HCR521, HCR522, HCR524 are high precision, rail-to-rail operational amplifiers that can be run from a single supply voltage 2.5V to 5.5V(±1.25V to ±2.75V). Supply voltages higher than 7V(absolute maximum) can permanently damage the amplifier. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. Good layout practice mandates use of a 0.1μF capacitor place closely across the supply pins.

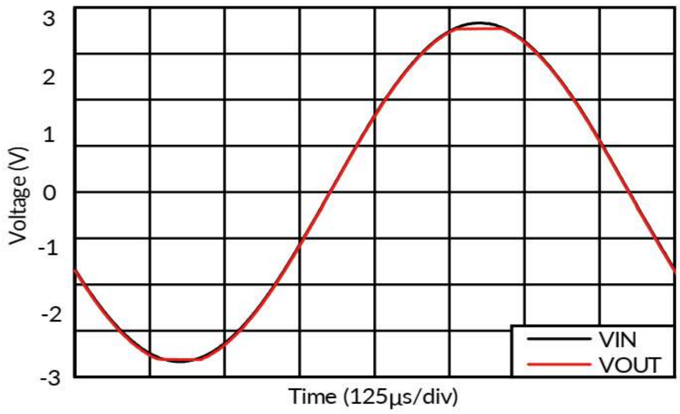


Figure 17. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition

Phase Reversal Protection

The HCR521/HCR522/HCR524 family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the HCR521/HCR522/HCR524 prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in figure 17.

EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this document provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier.

Detailed Description(con)

EMI Rejection Ratio (EMIRR)

In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input pin can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input pin with no complex interactions from other components or connecting PCB traces.

The EMIRR IN+ of the HCR521/HCR522/HCR524 is plotted versus frequency in Figure 18. If available, any dual and quad operational amplifier device versions have approximately identical EMIRR IN+ performance. The HCR521/HCR522/HCR524 unity-gain bandwidth is 3.7MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

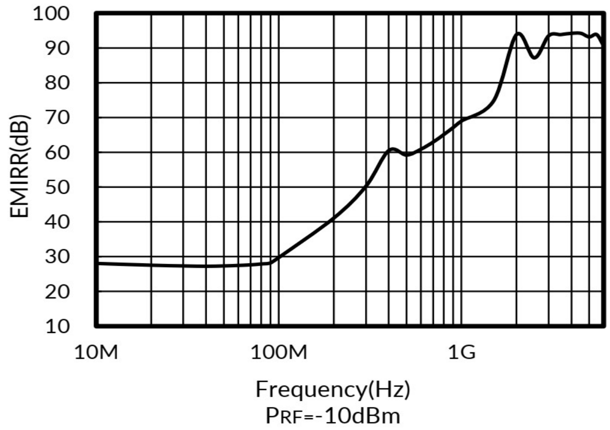


Figure 18. HCR521/HCR522/HCR524 EMIRR vs Frequency

EMIRR IN+ Test Configuration

Figure 19 shows the circuit configuration for testing the EMIRR IN+. RF source is connected to the operational amplifier noninverting input pin using a transmission line. The operational amplifier is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM).

A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting dc offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy.

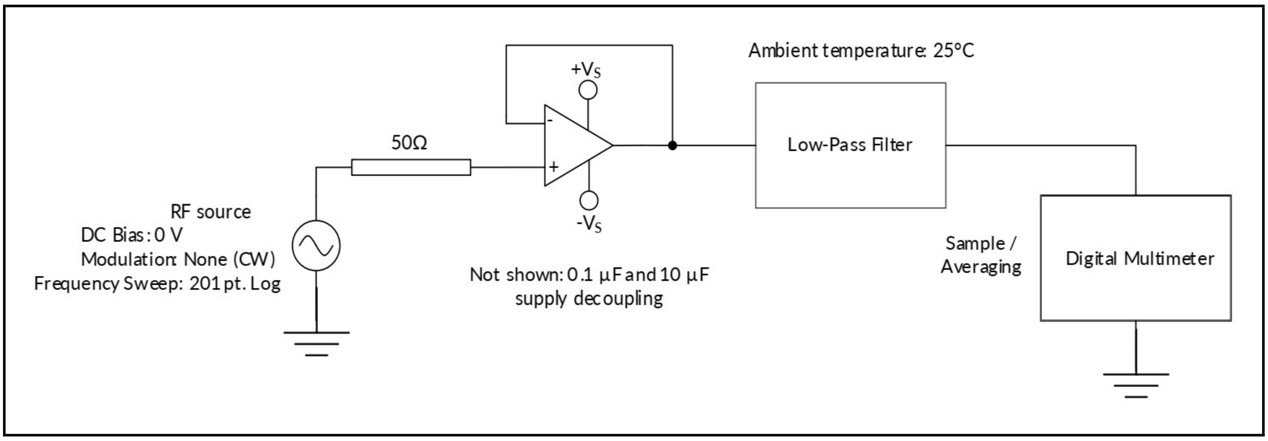


Figure 19. EMIRR IN+ Test Configuration Sche matic

3.6MHz, Low Noise Rail-to-Rail I/O CMOS Operational Amplifier

Application Note

The HCR521/HCR522/HCR524 are high precision, rail-to-rail operational amplifiers that can be run from a single-supply voltage 2.5V to 5.5V (±1.25V to ±2.75V). Supply voltages higher than 7V(absolute maximum) can permanently damage the amplifier. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. Good layout practice mandates use of a 0.1μF capacitor place closely across the supply pins.

Typical Applications

25-kHz Low-pass Filter

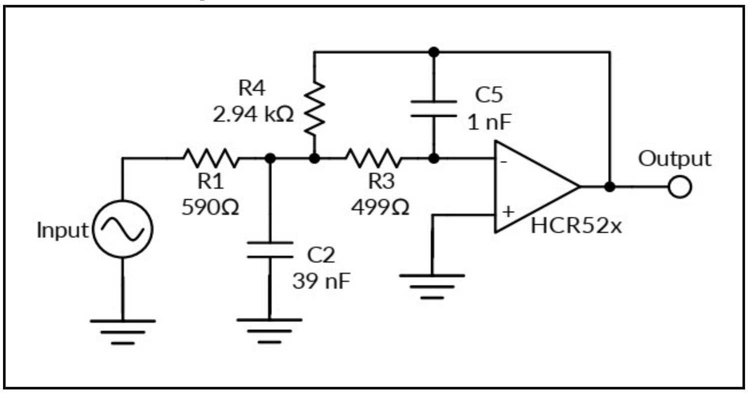


Figure 20. 25-kHz Low-pass Filter

Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing.

The HCR521/HCR522/HCR524 devices are ideally suited to construct high-speed, high-precision active filters. Figure 20 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband

Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 20. Use Equation 1 to calculate the voltage transfer function.

$$\frac{Output}{Input}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

$$Gain = \frac{R_4}{R_1} \quad (2)$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)}$$

Application Curve

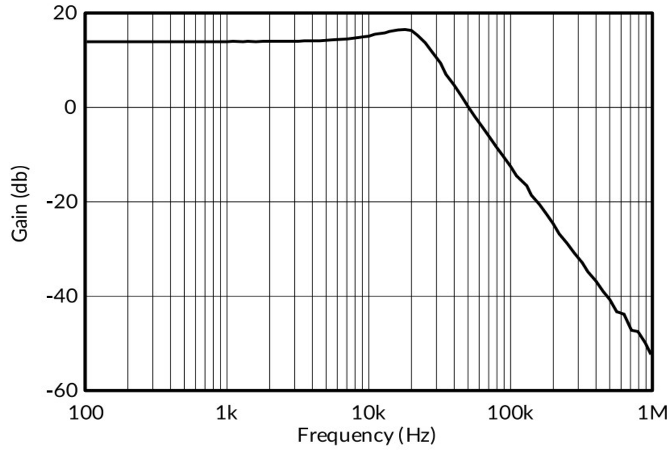


Figure 21. Low-Pass Filter Transfer Function

Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI susceptibility.

Layout Example

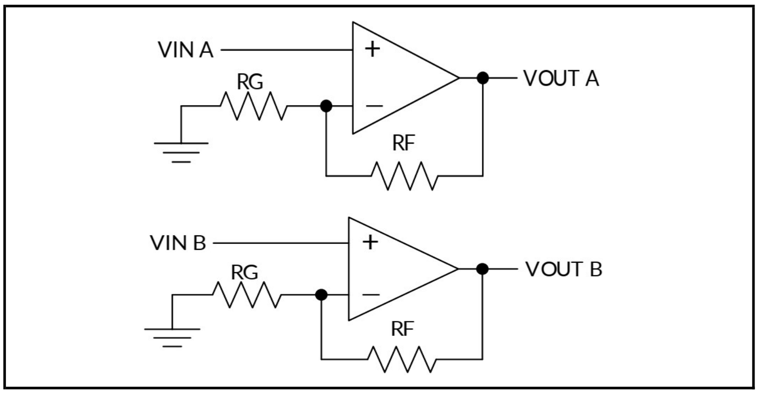
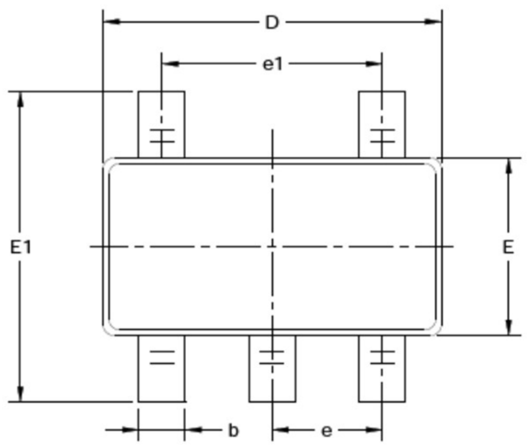
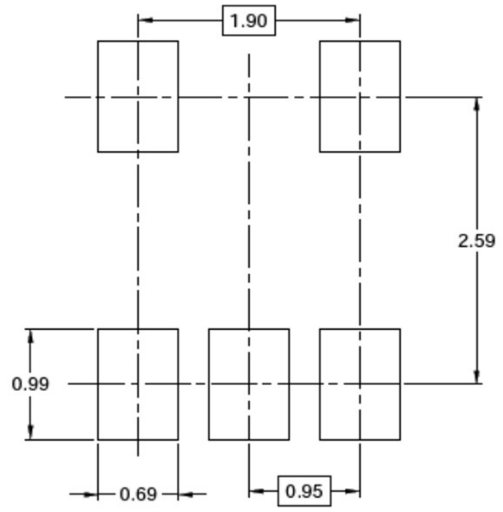


Figure 22. Schematic Representation

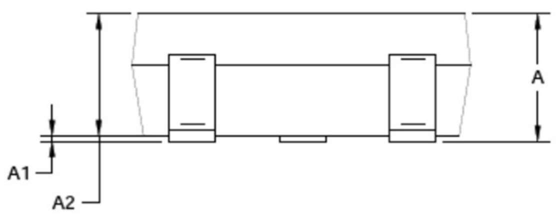
Mechanical Dimensions

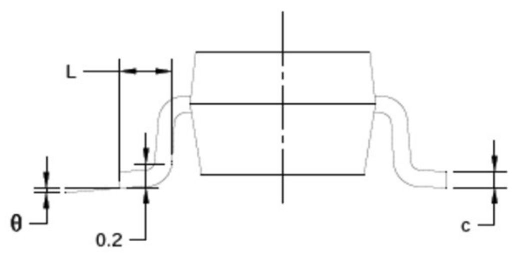
M5: SOT23-5 package





RECOMMENDED LAND PATTERN (Unit: mm)



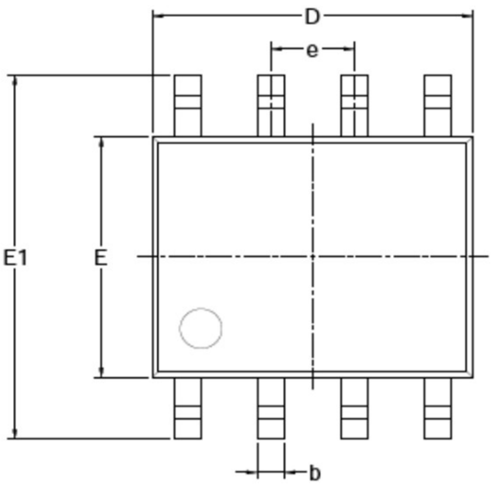


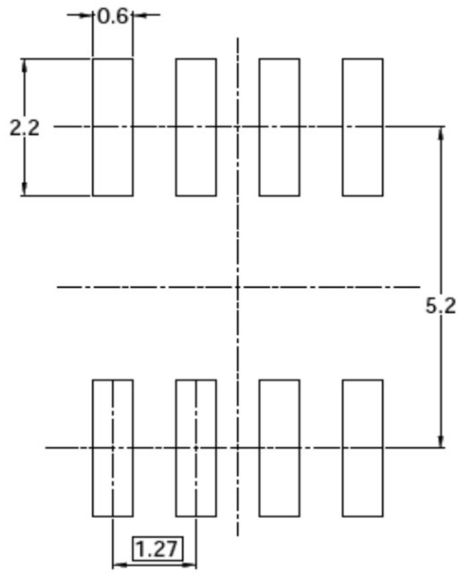
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.900 BSC		0.075 BSC	
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

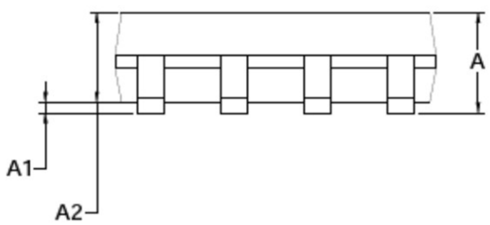
Mechanical Dimensions(Con.)

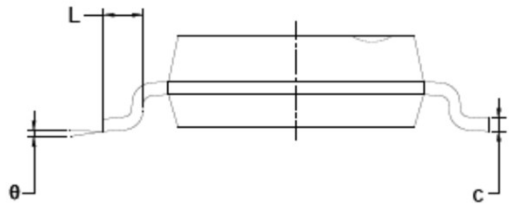
M8: SOIC-8(SOP-8) Package





RECOMMENDED LAND PATTERN (Unit: mm)



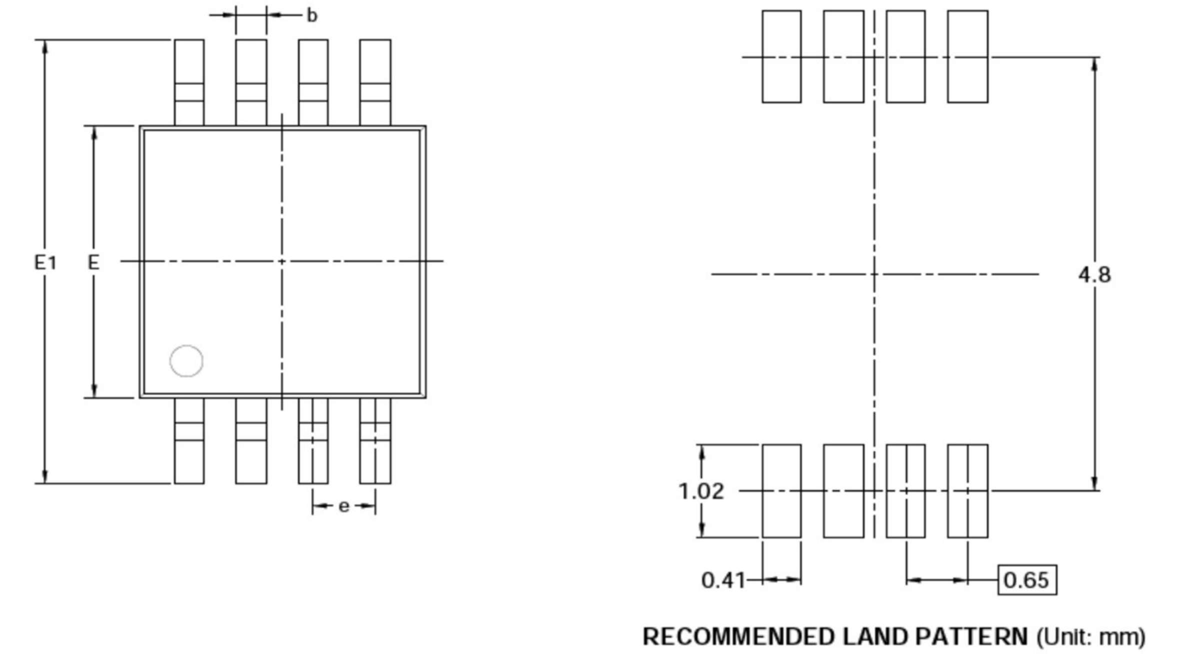


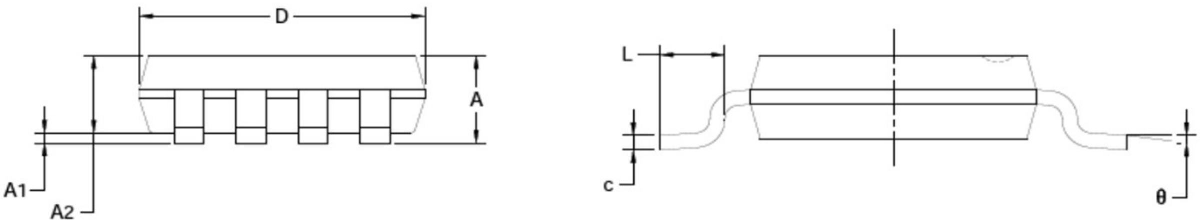
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

Mechanical Dimensions(Con.)

SM8: MSOP-8 Package



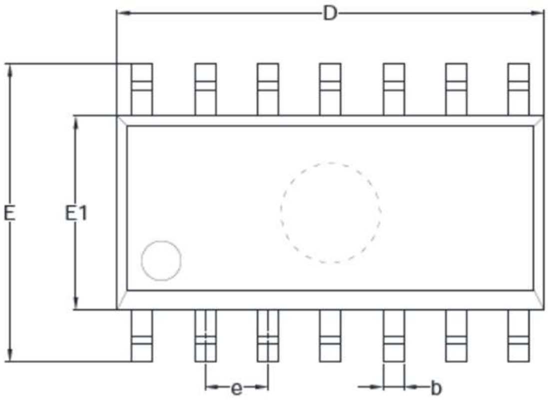


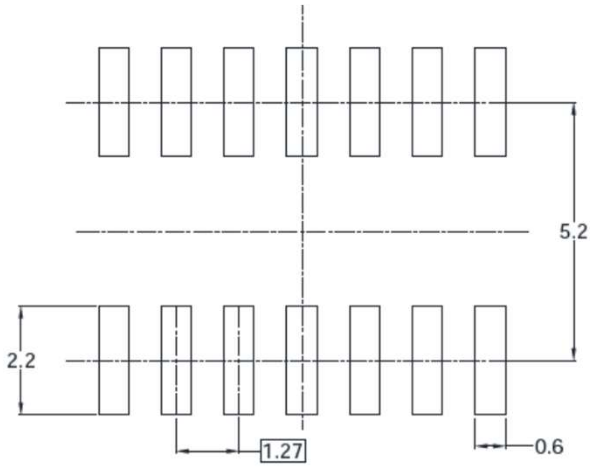
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

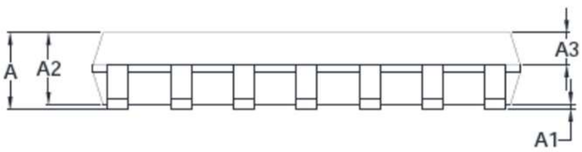
Mechanical Dimensions(Con.)

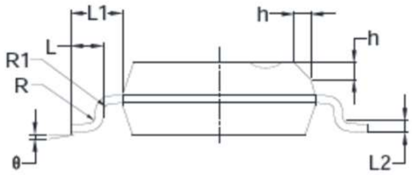
M14: SOIC-14 Package





RECOMMENDED LAND PATTERN (Unit: mm)



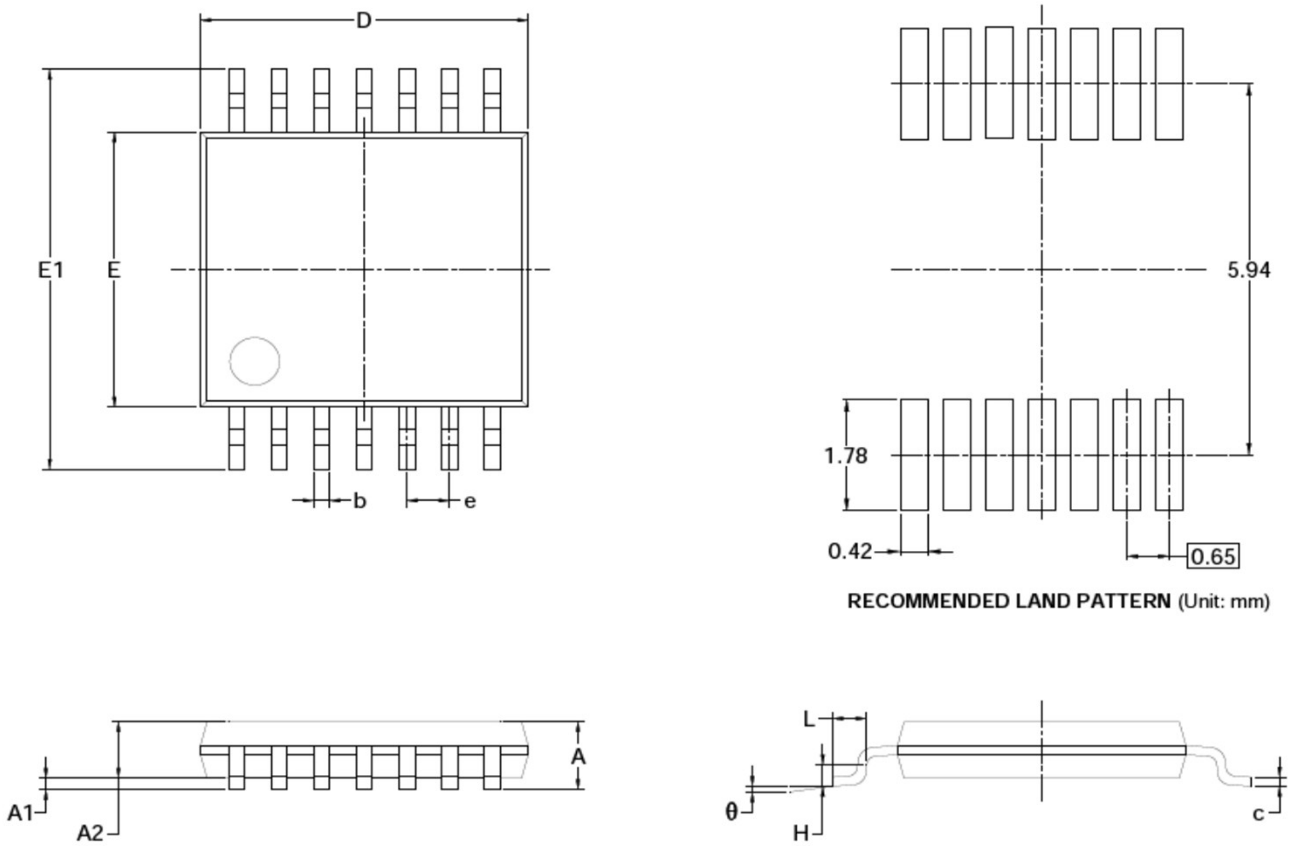


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.049	0.065
A3	0.55	0.75	0.022	0.030
b	0.36	0.49	0.014	0.019
D	8.53	8.73	0.336	0.344
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.45	0.80	0.018	0.032
L1	1.04 REF		0.040 REF	
L2	0.25 BSC		0.01 BSC	
R	0.07		0.003	
R1	0.07		0.003	
h	0.30	0.50	0.012	0.020
θ	0°	8°	0°	8°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

Mechanical Dimensions(Con.)

TSP14: TSSOP-14 Package



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

NOTES:
1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.