8-bit Serial-in, Serial or parallel-out shift register with output latches; 3-state

Features

* Input levels:
  For HCR74HC595: CMOS level
  For HCR74HCT595: TTL level
* 8-bit serial input
* 8-bit serial or parallel output
* Storage register with 3-state outputs
* Shift register with direct clear
* 100MHz (typical) shift out frequency
* Specified from -40'C to +85'C
* Packaging information:SOIC-16/TSSOP16
* ESD Protection:
  HBM EIA/JESD22-A114-A exceeds 2000V
  MM EIA/JESD22-A115-A exceeds 200V

Applications

* Serial-to-parallel data conversion
* Remote control holding register

General Description

The HCR74HC/HCT595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7') to enable cascading and an asynchronous reset $\overline{MR}$ input. A LOW on $\overline{MR}$ will reset the shift register. Data is shifted on the LOW-to HIGH transitions of the SH_CP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the ST_CP input.If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers. Inputs include clamp diodes, This enables the use of current limiting resistors to interface inputs to voltages in excess of VCC.

TSSOP-16

SOIC-16(SOP16)

Figure 1. Package Type of HCR74HC/HCT595

8-bit Serial-in, Serial or parallel-out shift register with output latches; 3-state

Pin Configuration

Top View TSSOP-16 and SOIC-16(SOP-16)

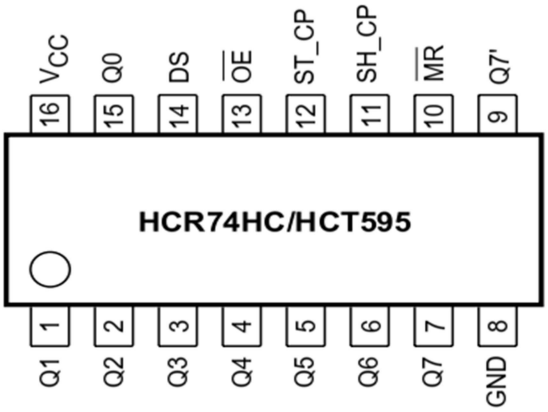


Figure 2. Pin Configuration of HCR74HC/HCT595 (Top View)

Pin Function Table

Pin TSSOP-16 SOP-16	NAME	FUNCTION
1	Q1	Parallel data output
2	Q2	Parallel data output
3	Q3	Parallel data output
4	Q4	Parallel data output
5	Q5	Parallel data output
6	Q6	Parallel data output
7	Q7	Parallel data output
8	GND	Ground(0V).
9	Q7'	Serial data output
10	$\overline{MR}$	master reset (active LOW)
11	SH_CP	shift register clock input
12	ST_CP	storage register clock input
13	$\overline{OE}$	Output enable input (active LOW)
14	DS	serial data input
15	Q0	Parallel data output
16	VCC	Positive supply voltage

8-bit Serial-in, Serial or parallel-out shift register with output latches; 3-state

Ordering Information

HCR74HC/HCT595

Circuit Type

TR : Tape and Reel
BP: Back&Packe

Package:
M16: SOIC-16
TSP16:TSSOP-16

Ordering Code

Part Number	Marking note1	Temperature Range	Package	Quantity per Reel
HCR74HC595M16TR	HCR74HC595xx	-40'C to +85'C	SOIC-16	4K/TR
HCR74HC595M16BP	HCR74HC595xx	-40'C to +85'C	SOIC-16	10K/Box
HCR74HC595TSP16TR	HCR74HC595xx	-40'C to +85'C	TSSOP-16	4K/TR
HCR74HC595TSP16BP	HCR74HC595xx	-40'C to +85'C	TSSOP-16	9.2K/Box
HCR74HCT595M16TR	HCR74HCT595xx	-40'C to +85'C	SOIC-16	4K/TR
HCR74HCT595M16BP	HCR74HCT595xx	-40'C to +85'C	SOIC-16	10K/Box
HCR74HCT595TSP16TR	HCR74HCT595xx	-40'C to +85'C	TSSOP-16	4K/TR
HCR74HCT595TSP16BP	HCR74HCT595xx	-40'C to +85'C	TSSOP-16	9.2K/Box

note 1. the "xx" is date code

QUICK REFERENCE DATA

GND=0V, Tamb=25'C, tr=tf=6ns

Parameter	Symbol	CONDITIONS	TYPICAL		Unit
			74HC	74HCT	
Propagation Delay		CL=50pF; VCC=4.5V			
SH_CP to Q7'	t_{PHL}/t_{PLH}		19	25	ns
SH_CP to Qn			20	24	ns
$\overline{MR}$ to Q7'			100	52	ns
Maximum Clock Frequency SH_CP and ST_CP	f_{max}		100	57	MHz
Input Capacitance	C_I	I_{OUT}	3.5	3.5	pF
Power Dissipation capacitance per package	C_{PD}	note1 and 2	115	130	pF

Note 1: C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_D)$ where:

fi = input frequency in MHz;

fo = output frequency in MHz;

CL = output load capacitance in pF;

VCC = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_D)$ = sum of the output.

2: For HCR74HC595 the condition is VI = GND to VCC.

For HCR74HCT595 the condition is VI = GND to VCC-1.5V.

8-bit Serial-in, Serial or parallel-out shift register with output latches; 3-state

FUNCTION TABLE

See note 3.

INPUT					OUTPUT		FUNCTION
SH_CP	ST_CP	$\overline{OE}$	$\overline{MR}$	DS	Q7'	Qn	
X	X	L	L	X	L	n.c.	a LOW level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel output in high-impedance OFF-state
↑	X	L	H	H	Q6'	n.c.	logic high level shifted into shift register stage 0; contents of all shift register stages shifted through, e.g. Previous state pf stage 6 (internal Q6') appears on the serial output (Q7')
X	↑	L	H	X	n.c.	Qn'	contents of shift register stages (internal Qn') are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6'	Qn'	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

Note 3: H = HIGH voltage lelvel;

L = LOW voltage level;

↑ = LOW-to-HIGH transition;

↓ = HIGH-to-LOW transition;

Z = high-impedance OFF-state;

n.c. = no change;

X = don't care.

LOGIC SYMBOL

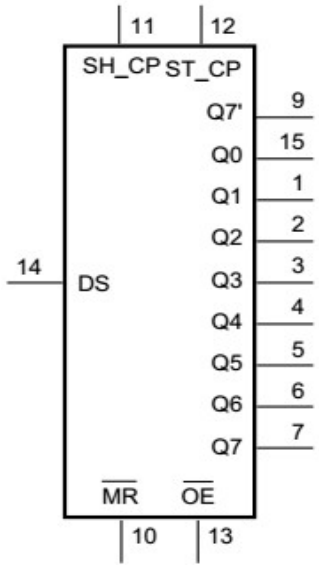


Figure 3. Logic Symbol

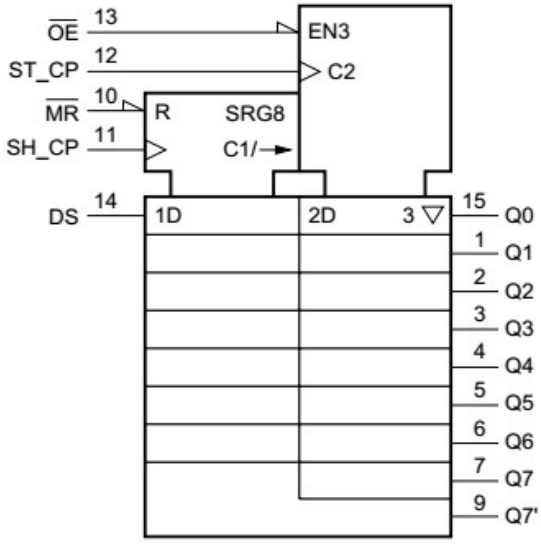


Figure 4. IEC Logic Symbol

8-bit Serial-in, Serial or parallel-out shift register with output latches; 3-state

FUNCTIONAL DIAGRAM

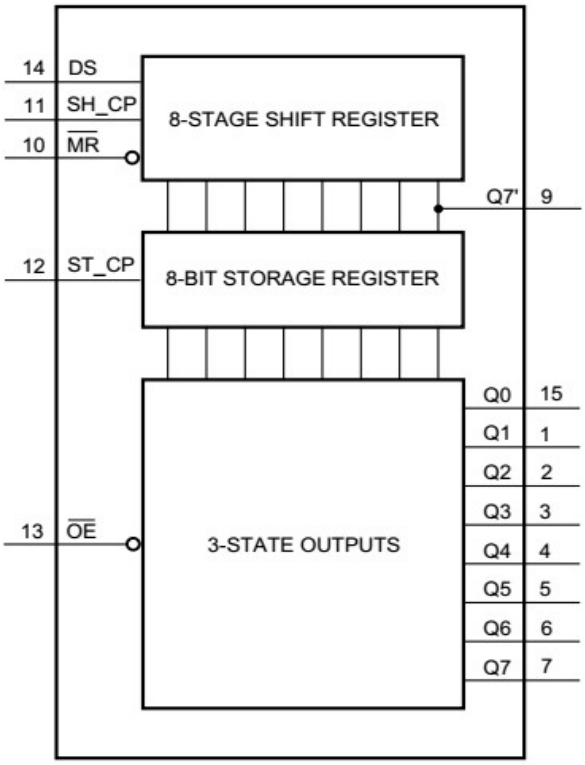


Figure 5. Functional Diagram

LOGIC DIAGRAM

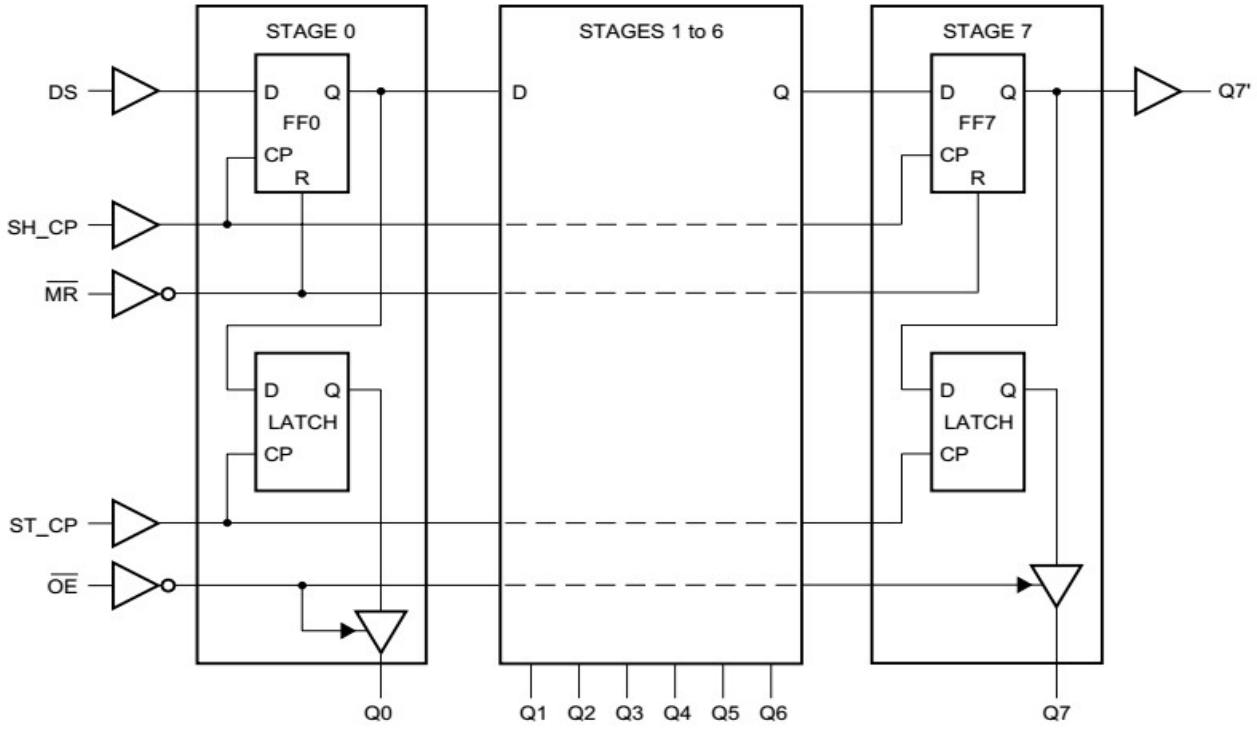


Figure 6-1. Logic Diagram

LOGIC DIAGRAM(con.)

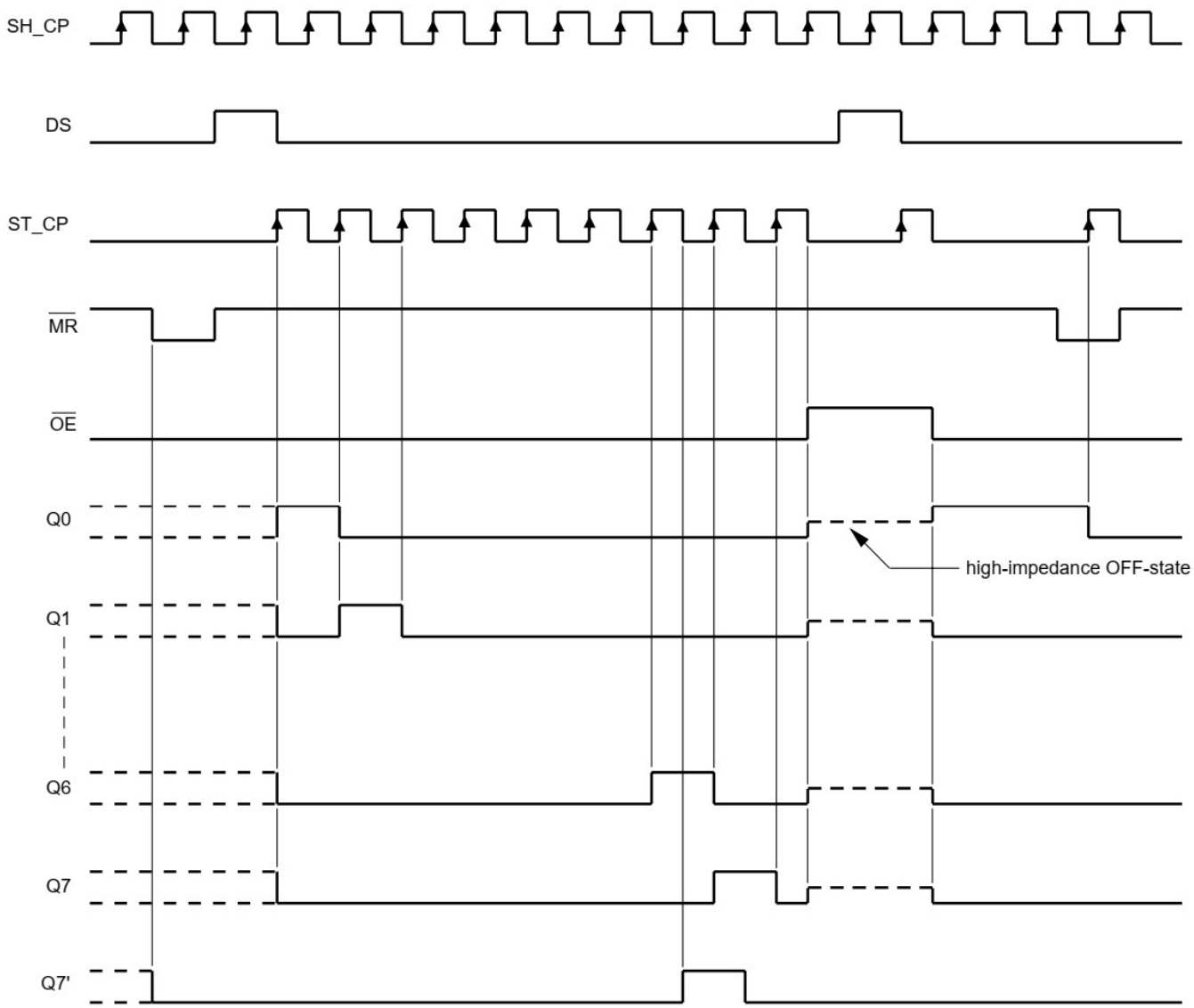


Figure 6-2. Timing Diagram

ELECTRICAL PARAMETER

Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Supply Voltage	V_{CC}	-	-0.5	-	+7.0	V
Input Clamping Current	I_{IK}	V_I<-0.5V to V_I>V_{CC}+0.5V	-	-	±20	mA
Output Clamping Current	I_{OK}	V_O<-0.5V to V_O>V_{CC}+0.5V	-	-	±20	mA
Output Source or Sink Current	I_O	V_O=-0.5V to V_{CC}+0.5V				
		Q7' standard output	-	-	±25	mA
		Qn bus driver outputs	-	-	±35	mA
VCC or GND Current	I_{CC},I_{GND}	V_O<-0.5V to V_O>V_{CC}+0.5V	-	-	±70	mA
Storage temperature	T_{stg}		-65	-	+150	'C
Power Dissipation	P_{tot}	Tamb=-40 to +125'C; note 4	-	-	500	mW

Note 4: For SOIC-16 pacakges: above 70'C derate linearly with 8mW/K.
For TSSOP-16 pacakges: above 60'C derate linearly with 5.5mW/K.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	UNIT
HCR74HC595						
Supply Voltage	V_{CC}		2.0	5.0	6.0	V
Input Voltage	V_I		0	-	V_{CC}	V
Output Voltage	V_O		0	-	V_{CC}	V
Ambient temperature	T_{amb}		-40	-	+85	'C
Input transition rise and fall time	Δt/ΔV	V_{CC}=2.0V	-	-	625	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	83	ns/V
HCR74HCT595						
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input Voltage	V_I		0	-	V_{CC}	V
Output Voltage	V_O		0	-	V_{CC}	V
Ambient temperature	T_{amb}		-40	-	+85	'C
Input transition rise and fall time	Δt/ΔV	V_{CC}=2.0V	-	-	-	ns/V
		V_{CC}=4.5V	-	1.67	139	ns/V
		V_{CC}=6.0V	-	-	-	ns/V

8-bit Serial-in, Serial or parallel-out shift register with output latches; 3-state

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Tamb=-40'C to +85'C, Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Test Condition		Min	Type	Max	Unit
		Other	Vcc(V)				
HCR74HC595							
High Level Input Voltage	V_{IH}		2.0	1.5	1.2	-	V
			4.5	3.15	2.4	-	
			6.0	4.2	3.2	-	
Low Level Input Voltage	V_{IL}		2.0	-	0.8	0.5	V
			4.5	-	2.1	1.35	
			6.0	-	2.8	1.8	
High Level Output Voltage	V_{OH}	V_I=V_{IH} or V_{IL}					
		all outputs I_O= -20uA	2.0	1.9	2.0	-	V
			4.5	4.4	4.5	-	
			6.0	5.9	6.0	-	
		Q7' standard output I_O= -4.0mA	4.5	3.84	4.32	-	V
		I_O= -5.2mA	6.0	5.34	5.81	-	
		Qn bus driver outputs I_O= -6.0mA	4.5	3.84	4.32	-	V
		I_O= -7.8mA	6.0	5.34	5.81	-	
LOW Level Output Voltage	V_{OL}	V_I=V_{IH} or V_{IL}					
		all outputs I_O= 20uA	2.0	-	0	0.1	V
			4.5	-	0	0.1	
			6.0	-	0	0.1	
		Q7' standard output I_O= 4.0mA	4.5	-	0.15	0.33	V
		I_O= 5.2mA	6.0	-	0.16	0.33	
		Qn bus driver outputs I_O= 6.0mA	4.5	-	0.15	0.33	V
		I_O= 7.8mA	6.0	-	0.16	0.33	
Input Leakage Current	I_{LI}	V_I=Vcc or GND	6.0	-	-	±1.0	uA
3-state output OFF-state current	I_{OZ}	V_I=V_{IH} or V_{IL}; V_O=Vcc or GND	6.0	-	-	±5.0	uA
Quiescent Supply Current	I_{CC}	V_I=Vcc or GND; I_O=0	6.0	-	-	80	uA
Input Capacitance	C_I	V_I=Vcc or GND; I_O=0	6.0	-	3.5	-	pF

8-bit Serial-in, Serial or parallel-out shift register with output latches; 3-state

ELECTRICAL CHARACTERISTICS(Con.)

DC Characteristics(Con.)

(Tamb=-40'C to +85'C, Voltages are referenced to GND(ground=0V), unless otherwise specified.)

Parameter	Symbol	Test Condition		Min	Type	Max	Unit
		Other	Vcc(V)				
HCR74HCT595							
High Level Input Voltage	V_{IH}		4.5 to 5.5	2.0	1.6	-	V
Low Level Input Voltage	V_{IL}		4.5 to 5.5	-	1.2	0.8	V
High Level Output Voltage	V_{OH}	V_I=V_{IH} or V_{IL}					
		all outputs; I_O= -20uA	-	4.4	4.5	-	V
		Q7' standard output I_O= -4.0mA	4.5	3.84	4.32	-	V
		Qn bus driver outputs I_O= -6.0mA	4.5	3.7	4.32	-	V
LOW Level Output Voltage	V_{OL}	V_I=V_{IH} or V_{IL}					
		all outputs I_O= 20uA	4.5	-	0	0.1	V
		Q7' standard output I_O= 4.0mA	4.5	-	0.15	0.33	V
		Qn bus driver outputs I_O= 6.0mA	4.5	-	0.16	0.33	V
Input Leakage Current	I_{LI}	V_I=Vcc or GND	5.5	-	-	±1.0	uA
3-state output OFF-state current	I_{OZ}	V_I=V_{IH} or V_{IL}; V_O=Vcc or GND	5.5	-	-	±5.0	uA
Quiescent Supply Current	I_{CC}	V_I=Vcc or GND; I_O=0	5.5	-	-	80	uA
additional supply current	ΔI_{CC}	per input pin;V_I=Vcc-2.1V, (pins MR, SH_CP, ST_CP, $\overline{OE}$)	4.5 to 5.5	-	150	675	uA
		other inputs at VCC or GND; IO=0A; (pin DS)	4.5 to 5.5	-	25	113	uA
Input Capacitance	C_I	V_I=Vcc or GND; I_O=0	5.5	-	3.5	-	pF

AC CHARACTERISTICS-1

(Tamb=25'C, voltages are referenced to GND (GND=0V); unless otherwise specified.)

Parameter	Symbol	Test Condition		Min	Type	Max	Unit
		WAVEFORMS	Vcc(V)				
HCR74HC595							
Propagation Delay SH_CP to Q7'	t_{PHL}, t_{PLH}	See Figure 8	2.0	-	52	160	ns
			4.5	-	19	32	ns
			6.0	-	15	27	ns
Propagation Delay ST_CP to Qn		See Figure 9	2.0	-	55	175	ns
			4.5	-	20	35	ns
			6.0	-	16	30	ns
Propagation Delay $\overline{MR}$ to Q7'	t_{PHL}	See Figure 11	2.0	-	47	175	ns
			4.5	-	17	35	ns
			6.0	-	14	30	ns
3-state output enable time $\overline{OE}$ to Qn	t_{PZH} /t_{PZL}	See Figure 12	2.0	-	47	150	ns
			4.5	-	17	30	ns
			6.0	-	14	26	ns
3-state output disable time $\overline{OE}$ to Qn	t_{PHZ} /t_{PLZ}	See Figure 12	2.0	-	41	150	ns
			4.5	-	15	30	ns
			6.0	-	12	27	ns
Shift clock pulse width HIGH or LOW	t_W	See Figure 8	2.0	75	17	-	ns
			4.5	15	6	-	ns
			6.0	13	5	-	ns
Storage clock pulse width HIGH or LOW	t_W	See Figure 9	2.0	75	11	-	ns
			4.5	15	4	-	ns
			6.0	13	3	-	ns
Master reset pulse width LOW	t_W	See Figure 11	2.0	75	17	-	ns
			4.5	15	6	-	ns
			6.0	13	5	-	ns
Set-up time DS to SH_CP	t_{SU}	See Figure 10	2.0	50	11	-	ns
			4.5	10	4	-	ns
			6.0	9	3	-	ns
Set-up time SH_CP to ST_CP	t_{SU}	See Figure 9	2.0	75	22	-	ns
			4.5	15	8	-	ns
			6.0	13	7	-	ns
Hold time DS to SH_CP	t_h	See Figure 10	2.0	+3	-6	-	ns
			4.5	+3	-2	-	ns
			6.0	+3	-2	-	ns
Removal time $\overline{MR}$ to SH_CP	t_{rem}	See Figure 11	2.0	+50	-19	-	ns
			4.5	+10	-7	-	ns
			6.0	+9	-6	-	ns

AC CHARACTERISTICS(Con.)

(Tamb=25'C, voltages are referenced to GND (GND=0V); unless otherwise specified.)

Parameter	Symbol	Test Condition		Min	Type	Max	Unit
		WAVEFORMS	Vcc(V)				
Maximum clock pulse frequency SH_CP or ST_CP	f_{max}	See Figure 8 and 9	2.0	9	30	-	MHz
			4.5	30	91	-	MHz
			6.0	35	108	-	MHz
Power dissipation capacitance	C_{PD}	all 9 outputs switching; f_I=1MHz; V_I=GND to VCC		-	115	-	pF
HCR74HCT595; Vcc=4.5V to 5.5V							
Propagation Delay SH_CP to Q7'	t_{PHL} /t_{PLH}	See Figure 8	4.5 to 5.5	-	25	42	ns
Propagation Delay ST_CP to Qn		See Figure 9	4.5 to 5.5	-	24	40	ns
HIGH to LOW Propagation Delay $\overline{MR}$ to Q7'	t_{PHL}	See Figure 11	4.5 to 5.5	-	23	40	ns
3-state output enable time $\overline{OE}$ to Qn	t_{PZH} /t_{PZL}	See Figure 12	4.5 to 5.5	-	21	35	ns
3-state output disable time $\overline{OE}$ to Qn	t_{PHZ} /t_{PLZ}	See Figure 12	4.5 to 5.5	-	18	30	ns
Shift clock pulse width HIGH or LOW	t_W	See Figure 8	4.5 to 5.5	16	6	-	ns
Storage clock pulse width HIGH or LOW	t_W	See Figure 9	4.5 to 5.5	16	5	-	ns
Master reset pulse width LOW	t_W	See Figure 11	4.5 to 5.5	20	8	-	ns
Set-up time DS to SH_CP	t_{SU}	See Figure 10	4.5 to 5.5	16	5	-	ns

AC CHARACTERISTICS(Con.)

(Tamb=25'C, voltages are referenced to GND (GND=0V); unless otherwise specified.)

Parameter	Symbol	Test Condition		Min	Type	Max	Unit
		WAVEFORMS	Vcc(V)				
Set-up time SH_CP to ST_CP	t_{SU}	See Figure 9	4.5 to 5.5	16	8	-	ns
Hold time DS to SH_CP	t_h	See Figure 10	4.5 to 5.5	+3	-2	-	ns
Removal time $\overline{MR}$ to SH_CP	t_{rem}	See Figure 11	4.5 to 5.5	10	-7	-	ns
Maximum clock pulse frequency SH_CP or ST_CP	f_{max}	See Figure 8 and 9	4.5 to 5.5	30	52	-	MHz
Power dissipation capacitance	C_{PD}	all 9 outputs switching; fI=1MHz; VI=GND to VCC-1.5V			130		pF

Note:

(1). Typical values are measured at nominal supply voltage.

(2). CPD is used to determine the dynamic power dissipation(PD in uW).

$P_D = C_{PD} X V_{CC}^2 X f_I + \Sigma(C_L X V_{CC}^2 X f_O)$ where:

f_I=input frequency in MHz;

f_O=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

$\Sigma(C_L X V_{CC}^2 X f_O)$=sum of outputs.

8-bit Serial-in, Serial or parallel-out shift register with output latches; 3-state

AC CHARACTERISTICS-2

(Tamb=-40' to +85'C, voltages are referenced to GND (GND=0V); unless otherwise specified.)

Parameter	Symbol	Test Condition		Min	Type	Max	Unit
		WAVEFORMS	Vcc(V)				
HCR74HC595							
Propagation Delay SH_CP to Q7'	t_{PHL}, t_{PLH}	See Figure 8	2.0	-	-	200	ns
			4.5	-	-	40	ns
			6.0	-	-	34	ns
Propagation Delay ST_CP to Qn		See Figure 9	2.0	-	-	220	ns
			4.5	-	-	44	ns
			6.0	-	-	37	ns
Propagation Delay $\overline{MR}$ to Q7'	t_{PHL}	See Figure 11	2.0	-	-	220	ns
			4.5	-	-	44	ns
			6.0	-	-	37	ns
3-state output enable time $\overline{OE}$ to Qn	t_{PZH} /t_{PZL}	See Figure 12	2.0	-	-	190	ns
			4.5	-	-	38	ns
			6.0	-	-	33	ns
3-state output disable time $\overline{OE}$ to Qn	t_{PHZ} /t_{PLZ}	See Figure 12	2.0	-	-	190	ns
			4.5	-	-	38	ns
			6.0	-	-	33	ns
Shift clock pulse width HIGH or LOW	t_W	See Figure 8	2.0	95	-	-	ns
			4.5	19	-	-	ns
			6.0	16	-	-	ns
Storage clock pulse width HIGH or LOW	t_W	See Figure 9	2.0	95	-	-	ns
			4.5	19	-	-	ns
			6.0	16	-	-	ns
Master reset pulse width LOW	t_W	See Figure 11	2.0	95	-	-	ns
			4.5	19	-	-	ns
			6.0	16	-	-	ns
Set-up time DS to SH_CP	t_{SU}	See Figure 10	2.0	65	-	-	ns
			4.5	13	-	-	ns
			6.0	11	-	-	ns
Set-up time SH_CP to ST_CP	t_{SU}	See Figure 9	2.0	65	-	-	ns
			4.5	13	-	-	ns
			6.0	11	-	-	ns
Hold time DS to SH_CP	t_h	See Figure 10	2.0	+3	-	-	ns
			4.5	+3	-	-	ns
			6.0	+3	-	-	ns
Removal time $\overline{MR}$ to SH_CP	t_{rem}	See Figure 11	2.0	65	-	-	ns
			4.5	13	-	-	ns
			6.0	11	-	-	ns

AC CHARACTERISTICS(Con.)

(Tamb=-40' to +85'C, voltages are referenced to GND (GND=0V); unless otherwise specified.)

Parameter	Symbol	Test Condition		Min	Type	Max	Unit
		WAVEFORMS	Vcc(V)				
Maximum clock pulse frequency SH_CP or ST_CP	f_{max}	See Figure 8 and 9	2.0	4.8	-	-	MHz
			4.5	24	-	-	MHz
			6.0	28	-	-	MHz
Power dissipation capacitance	C_{PD}	all 9 outputs switching; f_I=1MHz; V_I=GND to VCC		-	-	-	pF
HCR74HCT595; VCC=4.5V to 5.5V							
Propagation Delay SH_CP to Q7'	t_{PHL} /t_{PLH}	See Figure 8	4.5 to 5.5	-	-	53	ns
Propagation Delay ST_CP to Qn		See Figure 9	4.5 to 5.5	-	-	50	ns
HIGH to LOW Propagation Delay MR to Q7'	t_{PHL}	See Figure 11	4.5 to 5.5	-	-	50	ns
3-state output enable time $\overline{OE}$ to Qn	t_{PZH} /t_{PZL}	See Figure 12	4.5 to 5.5	-	-	44	ns
3-state output disable time $\overline{OE}$ to Qn	t_{PHZ} /t_{PLZ}	See Figure 12	4.5 to 5.5	-	-	38	ns
Shift clock pulse width HIGH or LOW	tw	See Figure 8	4.5 to 5.5	20	-	-	ns
Storage clock pulse width HIGH or LOW	tw	See Figure 9	4.5 to 5.5	20	-	-	ns
Master reset pulse width LOW	tw	See Figure 11	4.5 to 5.5	25	-	-	ns
Set-up time DS to SH_CP	t_{SU}	See Figure 10	4.5 to 5.5	20	-	-	ns

AC CHARACTERISTICS(Con.)

(Tamb=-40' to +85'C, voltages are referenced to GND (GND=0V); unless otherwise specified.)

Parameter	Symbol	Test Condition		Min	Type	Max	Unit
		WAVEFORMS	VCC(V)				
Set-up time SH_CP to ST_CP	t_{SU}	See Figure 9	4.5 to 5.5	20	-	-	ns
Hold time DS to SH_CP	t_h	See Figure 10	4.5 to 5.5	+3	-	-	ns
Removal time MR to SH_CP	t_{rem}	See Figure 11	4.5 to 5.5	13	-	-	ns
Maximum clock pulse frequency SH_CP or ST_CP	f_{max}	See Figure 8 and 9	4.5 to 5.5	24	-	-	MHz
Power dissipation capacitance	C_{PD}	all 9 outputs switching; fI=1MHz; VI=GND to VCC-1.5V		-	-	-	pF

Note:

(1). Typical values are measured at nominal supply voltage.

(2). CPD is used to determine the dynamic power dissipation(PD in uW).

$P_D=C_{PD}XV_{CC}^2$ X $f_I+\Sigma(C_LXV_{CC}^2$ X$f_O)$ where:

f_I=input frequency in MHz;

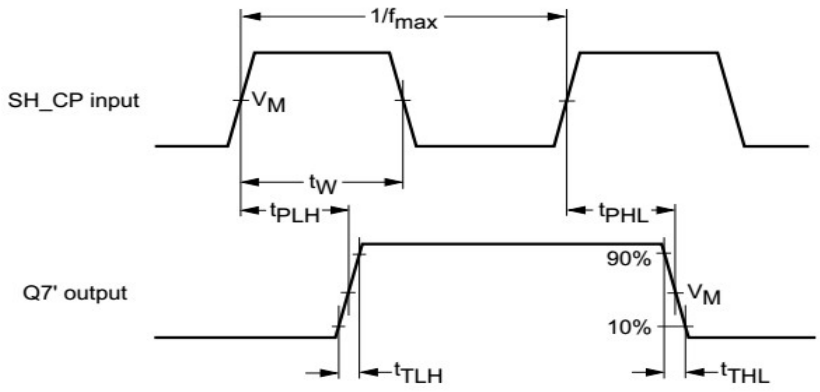
f_o=output frequency in MHz;

C_L=output load capacitance in pF;

V_{CC}=supply voltage in V;

$\Sigma(C_LXV_{CC}^2$ X$f_O)$=sum of outputs.

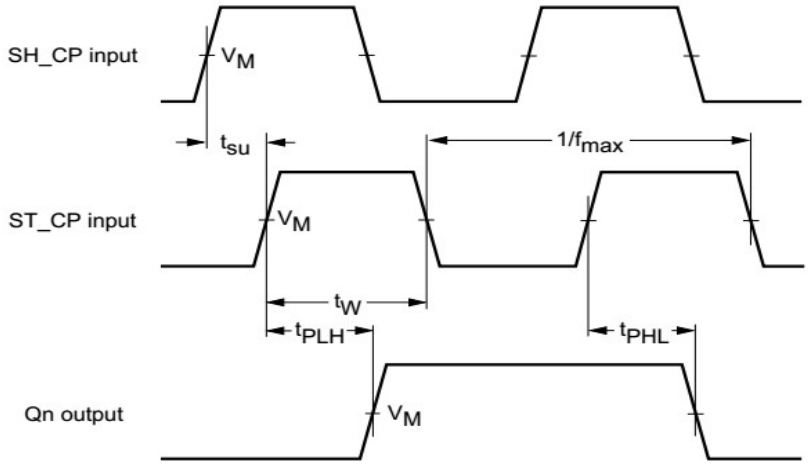
AC WAVEFORMS



HCR74HC/HCT595: V_M=50%; V_I=GND to V_{CC}

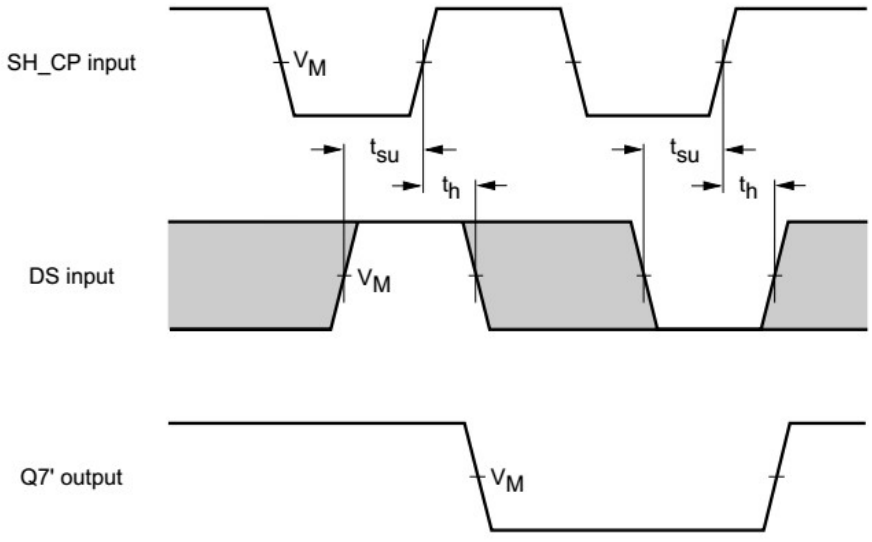
Figure 8. Waveforms showing the clock(SH_CP) to output (Q7') propagtion delays, the shift clock pulse and maximum shift clock frequency.

AC WAVEFORMS (Con.)



HCR74HC/HCT595: V_M=50%; V_I=GND to V_{CC}

Figure 9. Waveforms showing the storage clock(ST_CP) to output (Qn) propagtion delays, the storage clock pulse width and the shift clock to storage clock set-up time.

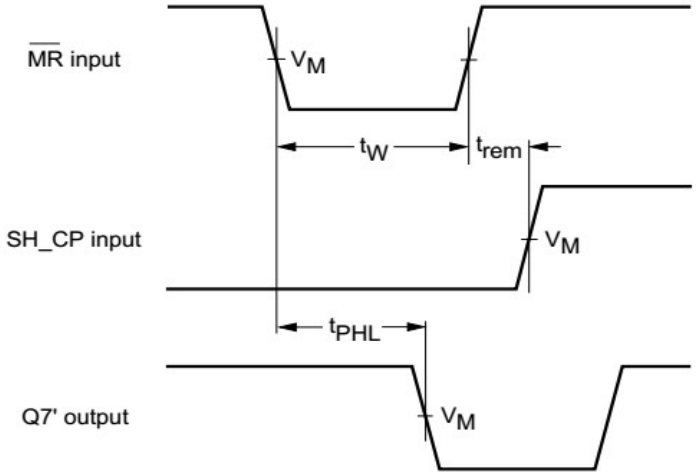


HCR74HC/HCT595: V_M=50%; V_I=GND to V_{CC}

Figure 10. Waveforms showing the data set-up and hold times for the DS input

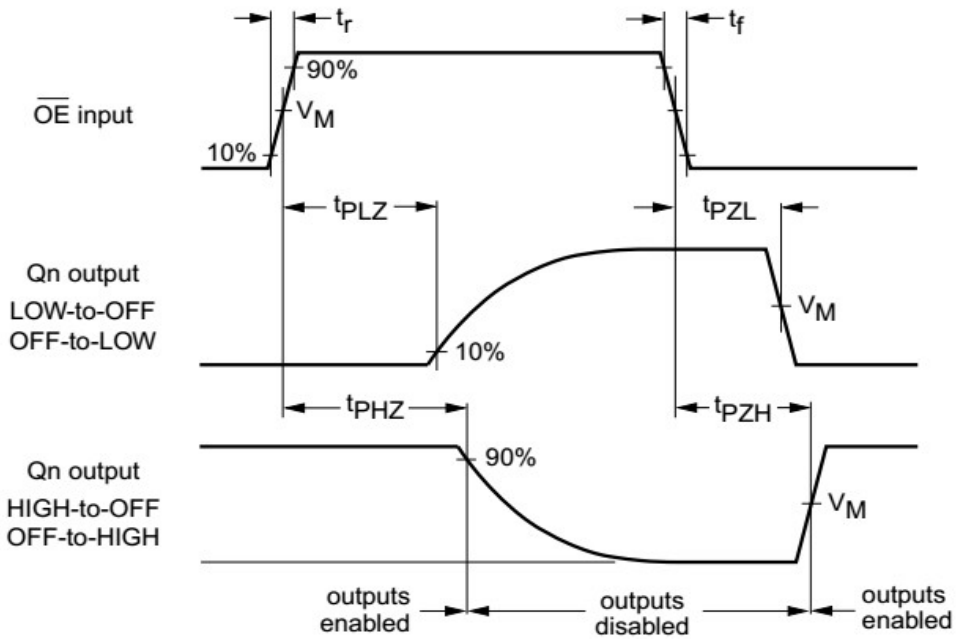
8-bit Serial-in, Serial or parallel-out shift register with output latches; 3-state

AC WAVEFORMS (Con.)



HCR74HC/HCT595: V_M=50%; V_I=GND to V_{CC}

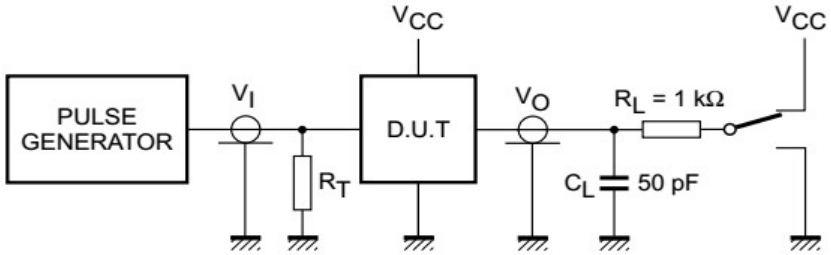
Figure 11. Waveforms showing the Master Reset($\overline{MR}$) pulse width, the master reset to output (Q7') propagation delay and the master reset to shift clock(SH_CP) removal time.



HCR74HC/HCT595: V_M=50%; V_I=GND to V_{CC}

Figure 12. Waveforms showing the 3-state enable and disable times for input $\overline{OE}$.

AC WAVEFORMS (Con.)



TEST	SWITCH
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

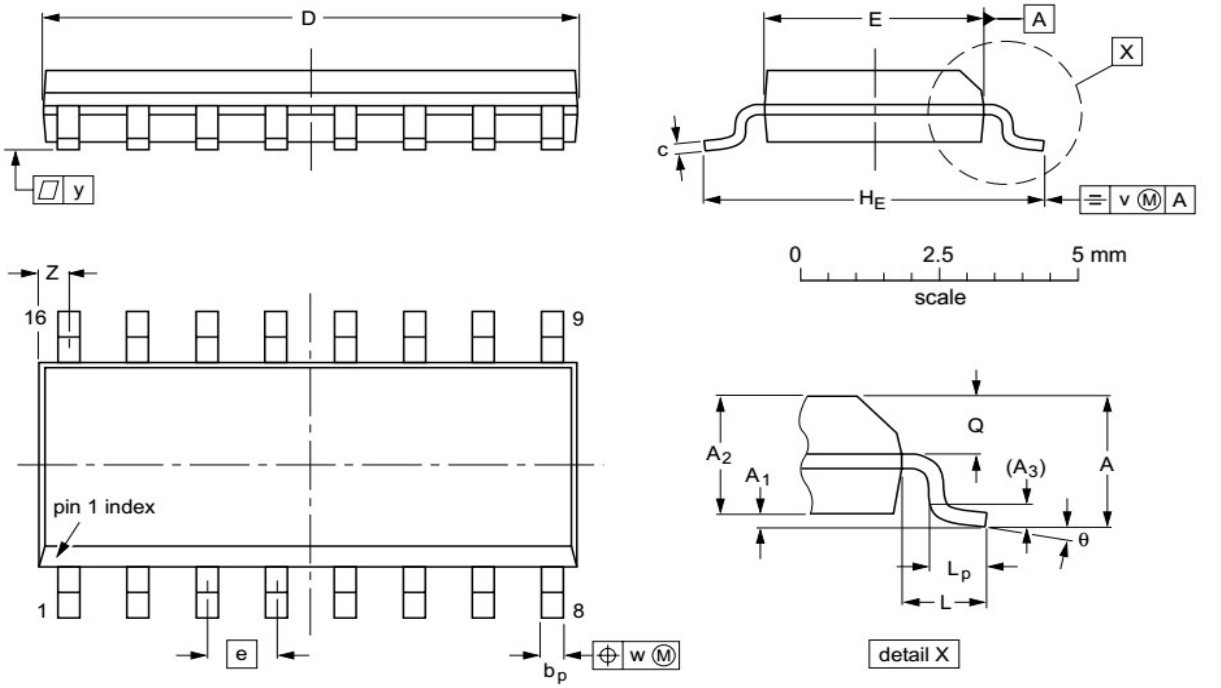
R_T = Termination resistance should be equal to the output impedance Zo of the pulse generator.

Figure 13. Test circuit for 3-state outputs.

MECHANICAL DIMENSIONS.

PKG: SOIC-16 (M16)

Unit:mm



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

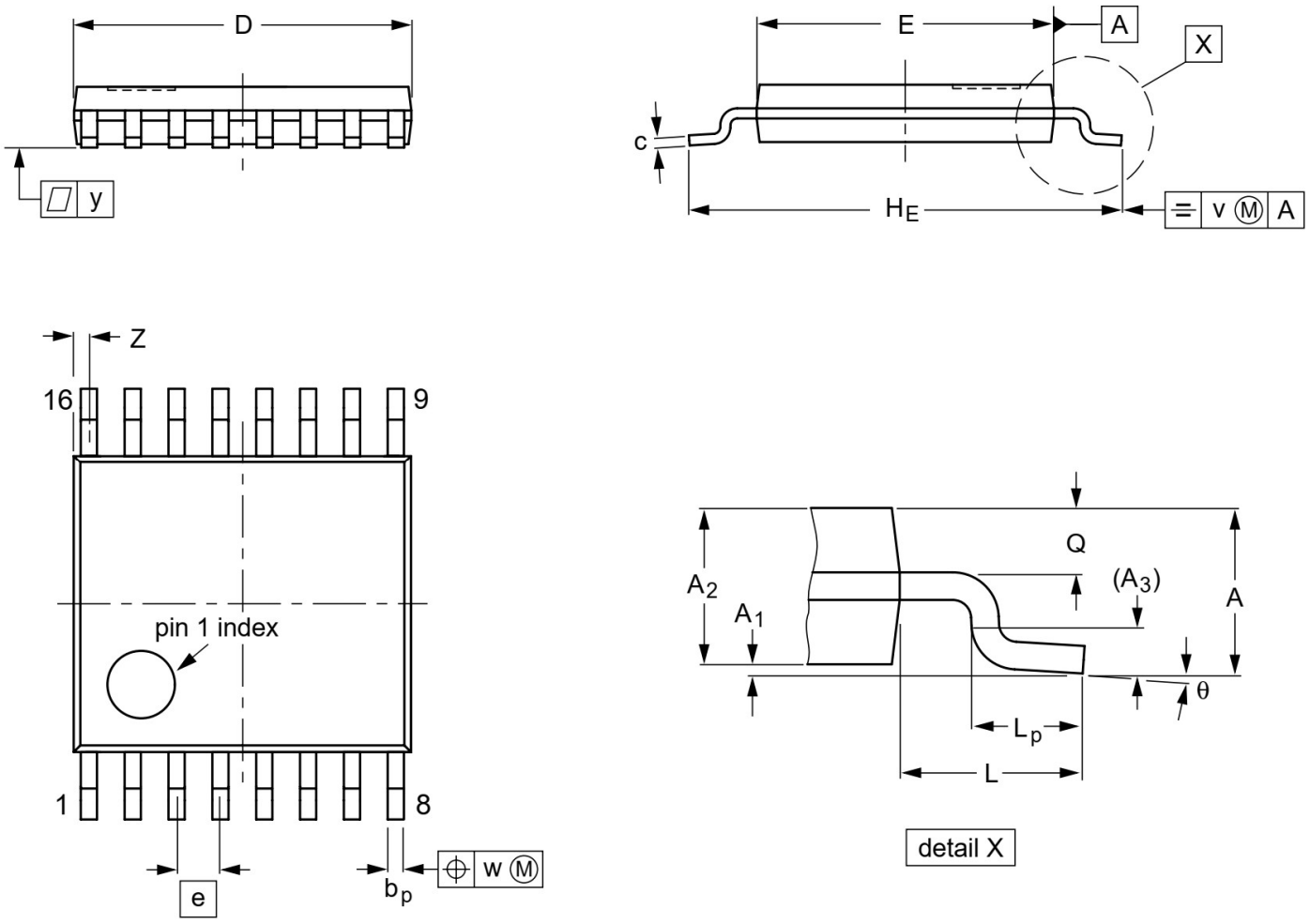
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

8-bit Serial-in, Serial or parallel-out shift register with output latches; 3-state

MECHANICAL DIMENSIONS(Con.)

PKG: TSSOP-16 (TSP16)

Unit:mm



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.