17V, 3A, 600kHz Synchronous Buck Converter

Features

- Up to 95% efficiency
- Input voltage range: 4.5V to 17V
- Output voltage range: 0.8V to 7V
- Continuous output current: 3A
- CCM switching frequency: 600kHz
- Reference voltage: 0.8V ±2% at 25°C
- Maximum duty cycle: 96%
- Integrated MOSFETs: 60mΩ and 35mΩ
- Low quiescent current: 500μA
- Low shutdown current: 5μA
- COT control
- Optional operation modes at light load:
  HCR3123D: Power Save Mode (PSM)
  HCR3123FD: Continuous Current Mode (CCM)
- Over current protection
- Short protection with hiccup mode
- Internal soft startup
- Thermal shutdown protection
- Built-in 1kΩ discharge resistor

General Description

The HCR3123D/HCR3123FD is a low EMI signature, synchronous, step-down, COT-mode converter with internal power MOSFETs. It offers a very compact solution to provide 3.0A continuous current over a wide input supply range, with excellent load and line regulation. HCR3123D/HCR3123FD achieves low EMI signature with well controlled switching edges. Fault condition protection includes programmable output over-voltage protection and thermal shutdown.

DCM/CCM mode operation provides very low output ripple voltage for noise sensitive applications. Switching frequency is internally set at 750kHz, allowing the use of small surface mount inductors and capacitors. Low output voltages are easily supported with the 0.8V feedback reference voltage.

The HCR3123D/HCR3123FD requires a minimal number of readily available external components and is available in a small package.

Applications

- Automotive entertainment
- Wireless and DSL modems
- Computer entertainment
- IoT applications
- Digital still and video cameras
- Portable instruments



PDFN-1.6×1.6-6L

Figure 1. Package Type of HCR3123D/HCR3123FD

Pin Configuration

PDFN-1.6×1.6-6L (Top View)

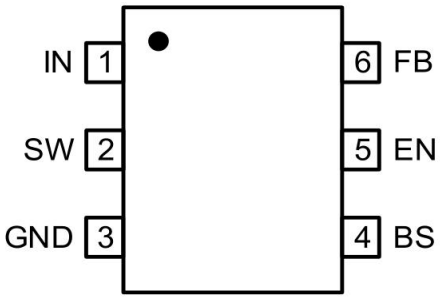
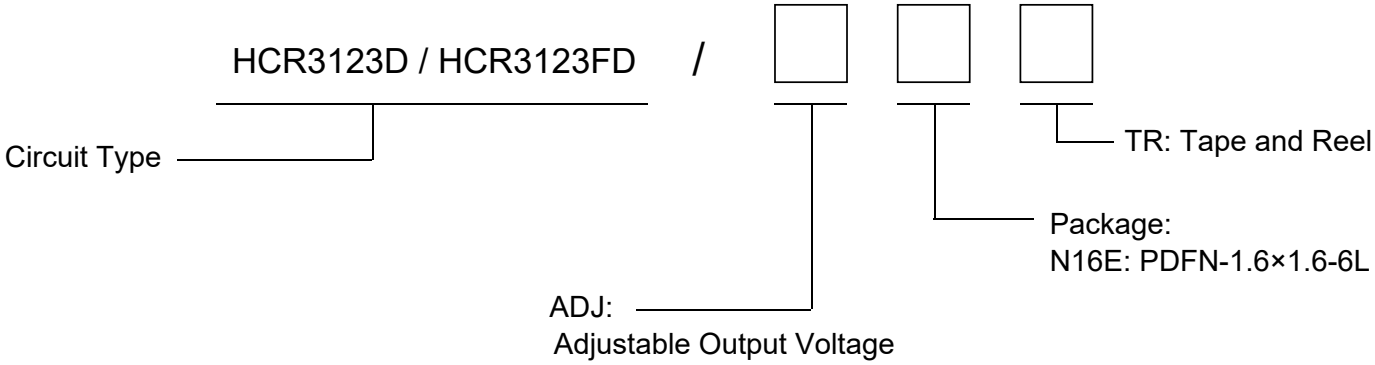


Figure 2. Pin Configuration of HCR3123D/HCR3123FD

Pin Function Table

Pin No.	Name	Function
1	IN	Power supply voltage input.
2	SW	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter to this pin.
3	GND	Ground pin.
4	BS	Supply input for the high-side NFET gate drive circuit. Connect a 0.1μF capacitor between BS and SW pins.
5	EN	Chip enable pin. Drive EN above 1.2V to turn on the part. Drive EN below 0.4V to turn it off.
6	FB	Feedback pin for the internal control loop. Connect this pin to an external feedback divider.

Ordering Information



Ordering Code

Part Number	Marking ID	Temperature Range	Package	Quantity per Reel
HCR3123D/ADJN16ETR	31213Dxx	−40 to +125°C	PDFN-1.6×1.6-6L	3000 pcs
HCR3123FD/ADJN16ETR	31213FDxx	−40 to +125°C	PDFN-1.6×1.6-6L	3000 pcs

Note: xx indicates the date code and trace code. Pb-free in tape and reel.

Device	Light-Load Operation
HCR3123D	Power Save Mode (PSM)
HCR3123FD	Continuous Current Mode (CCM)

Absolute Maximum Ratings

Over operating temperature range, unless otherwise noted. (1)

Parameter	Min.	Max.	Unit
V_{IN} voltage	−0.3	19	V
EN voltage	−0.3	19	V
SW voltage (DC)	−0.3	19	V
SW voltage (AC less than 10ns while switching)	−3	22	V
FB voltage	−0.3	6.5	V
BS voltage (vs. SW)	−0.3	5.5	V
Operating junction temperature, T_J	−40	150	°C
Storage temperature, T_{stg}	−65	150	°C
Lead temperature (soldering, 10sec.)	-	260	°C

Note (1): Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Note (2): All voltage values are with respect to the network ground terminal.

Recommended Operating Conditions

Parameter	Min.	Max.	Unit
V_{IN} voltage (V_{IN})	4.5	17	V
Output current (I_{OUT})	0	3	A
Operating junction temperature, T_J	−40	125	°C

Note (1): All limits are specified at room temperature (T_A = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

ESD Ratings and Thermal Information

Parameter	Description	Value	Unit
HBM	Human-body model, per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
CDM	Charged-device model, per JEDEC specification JESD22-C101 (2)	±500	V

Note (1): JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

Note (2): JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

Thermal Information

Thermal Metric	Description	PDFN-1.6×1.6-6L	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1) (2)	95	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.5	°C/W
$R_{\theta JB}$	Junction-to-board (bottom) thermal resistance	15.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.5	°C/W

Note (1): The package thermal impedance is calculated in accordance with JESD 51-7.

Note (2): Thermal resistances were simulated on a 4-layer JEDEC board.

Typical Application Circuit

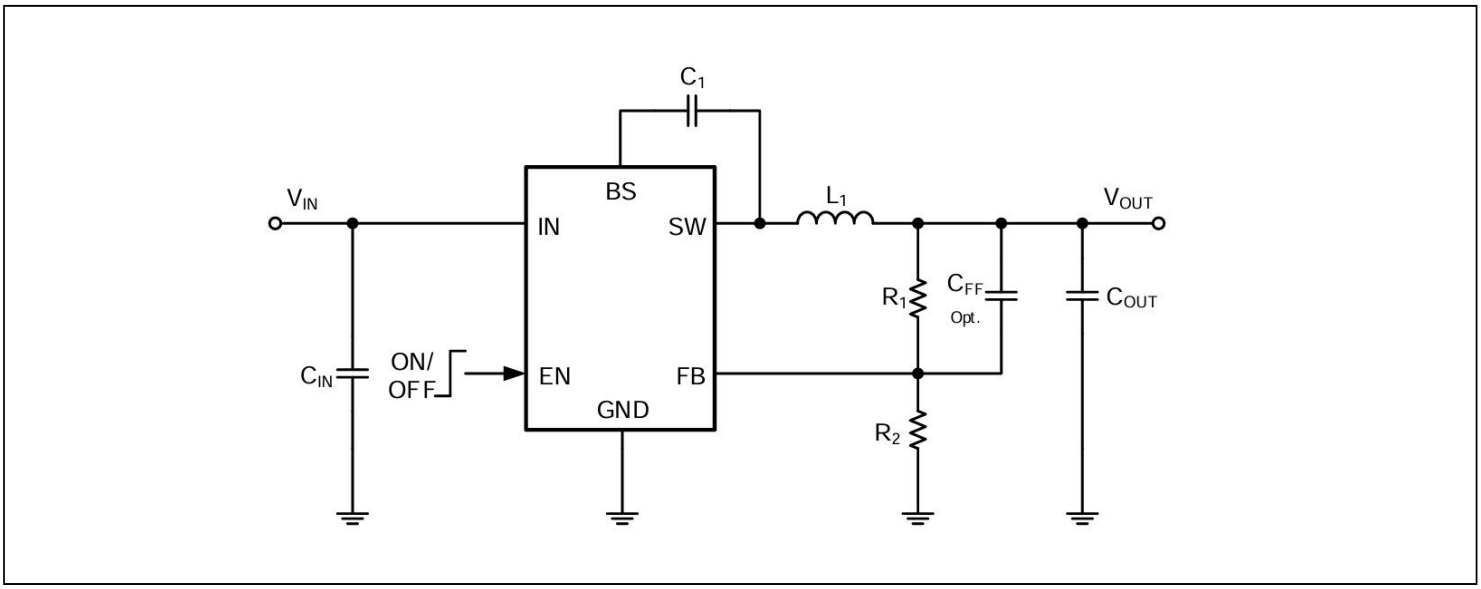


Figure 3. Typical Application Circuit

Functional Block Diagram

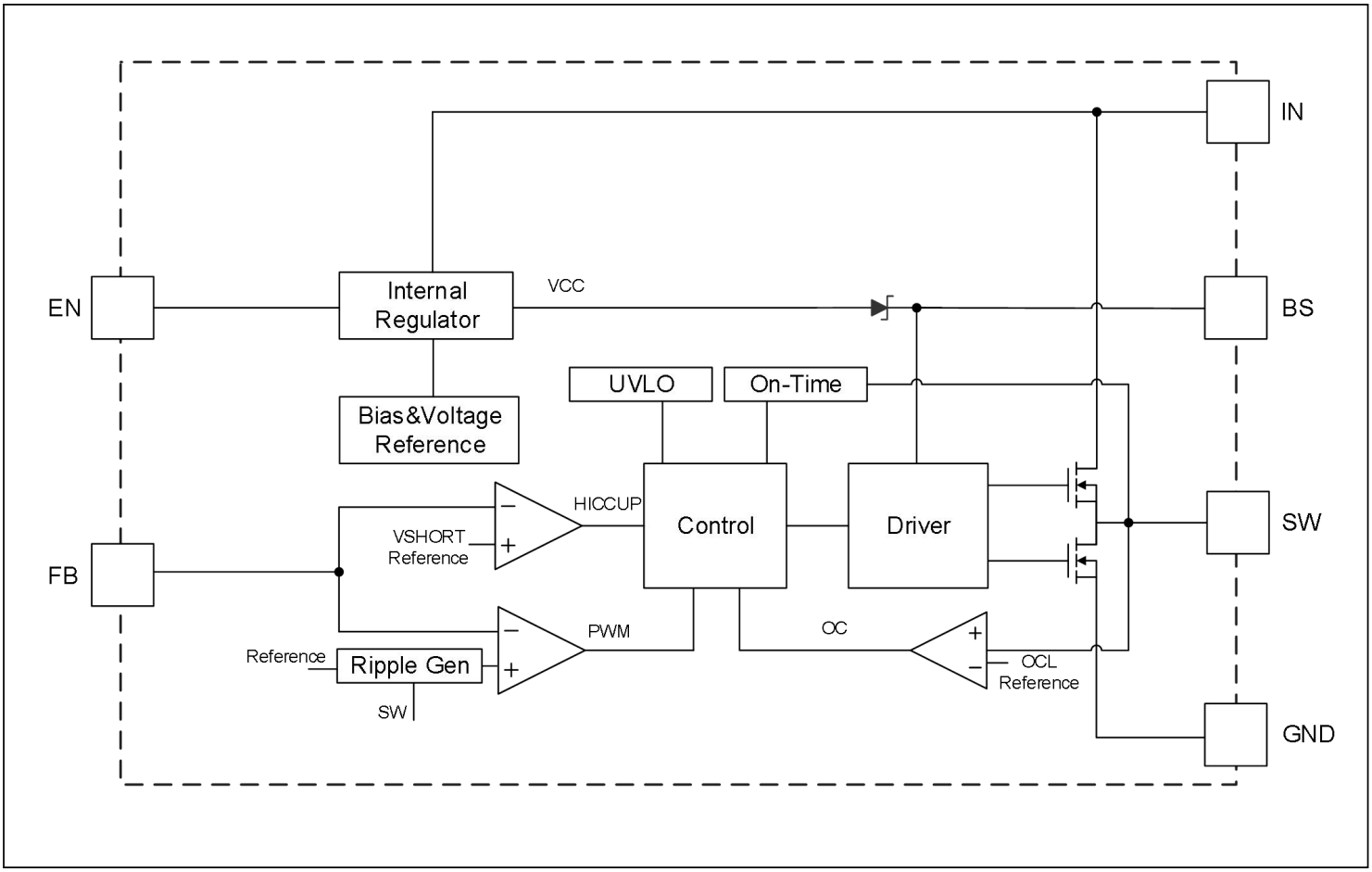


Figure 4. Functional Block Diagram

Electrical Characteristics

Typical at V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}	-	4.5	-	17	V
V_{IN} quiescent current	I_Q (HCR3123D)	No switching, V_{EN} = 12V, V_{FB} = V_{REF} × 105%, I_{OUT} = 0A	-	500	-	μA
V_{IN} quiescent current	$I_{STANDBY}$ (HCR3123FD)	Switching, V_{EN} = 12V, I_{OUT} = 0A, V_{OUT} = 3.3V	-	10	-	mA
Shutdown current	I_{SHDN}	V_{EN} = 0V	-	5	10	μA
V_{IN} UVLO rising threshold	$V_{UVLO(R)}$	V_{IN} rising	-	3.9	-	V
V_{IN} UVLO falling threshold	$V_{UVLO(F)}$	V_{IN} falling	-	3.5	-	V
V_{IN} UVLO hysteresis	$V_{UVLO(HYS)}$	-	-	0.4	-	V
V_{IN} OVP rising threshold	$V_{OVP(R)}$	V_{IN} rising	-	19	-	V
V_{IN} OVP hysteresis	$V_{OVP(HYS)}$	-	-	0.1	-	V
FB voltage	V_{FB}	T_J = 25°C	0.784	0.8	0.816	V
FB leakage current	$I_{FB(LkG)}$	T_J = 25°C	−100	0	100	nA
Switching frequency	F_{sw}	V_{OUT} = 1.5V, operation CCM	-	600	-	kHz

Electrical Characteristics (Continued)

Typical at V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Maximum duty cycle	D_{max}	-	-	-	96	%
Minimum on pulse width	$T_{ON(MIN)}$	-	-	90	-	ns
High-side switch current limit	$I_{HS(OC)}$	V_{IN} = 12V, V_{FB} = 90%	-	5	-	A
Low-side switch current limit	$I_{LS(OC)}$	V_{IN} = 12V, V_{FB} = 90%	-	4	-	A
High-side MOS on-resistance	$R_{DSON(HS)}$	I_{SW} = 100mA	-	60	-	mΩ
Low-side MOS on-resistance	$R_{DSON(LS)}$	I_{SW} = 100mA	-	35	-	mΩ
EN rising threshold	$V_{EN(R)}$	4.5V ≤ V_{IN} ≤ 17V	1.2	-	-	V
EN falling threshold	$V_{EN(F)}$	4.5V ≤ V_{IN} ≤ 17V	-	-	0.4	V
EN hysteresis	$V_{EN(HYS)}$	-	-	0.1	-	V
Soft start	T_{ss}	10% × V_{OUT} to 90% × V_{OUT}	-	600	-	μs
Over-temperature protection	T_{SD}	-	-	160	-	°C
Over-temperature protection hysteresis	ΔT_{SD}	-	-	30	-	°C
Output discharger resistance	-	V_{IN} = 12V, EN = 0V	-	1000	-	Ω

Typical Characteristics

Test conditions: T_A = 25°C, V_{IN} = 12V, V_{OUT} = 1.2V, unless otherwise noted.

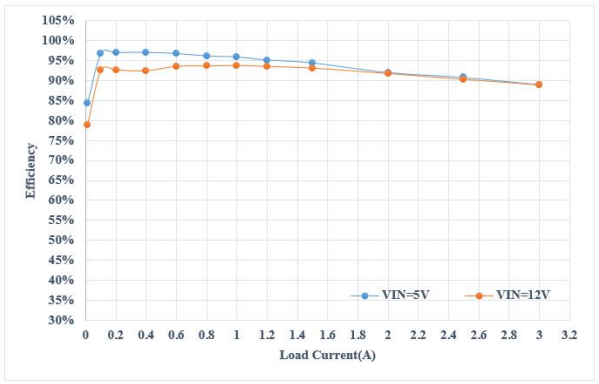


Figure 5. 3.3V Output Efficiency

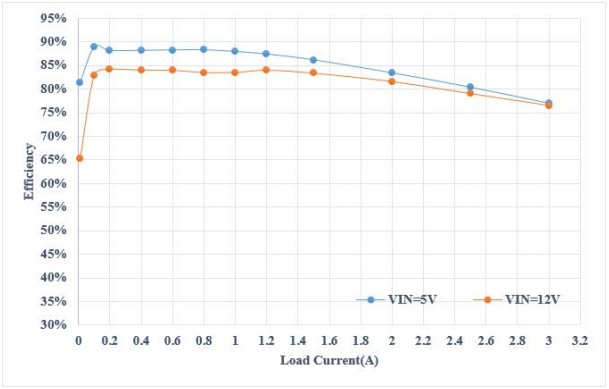


Figure 6. 1.2V Output Efficiency

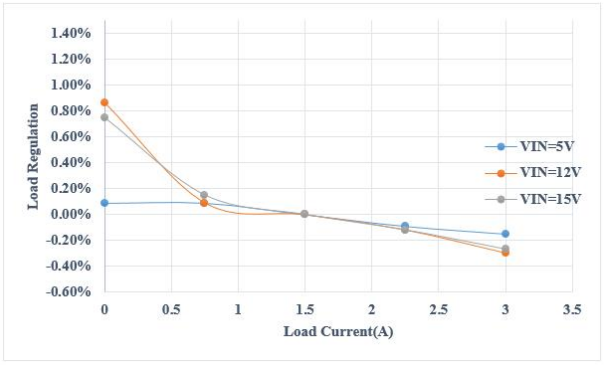


Figure 7. 3.3V Output Load Regulation

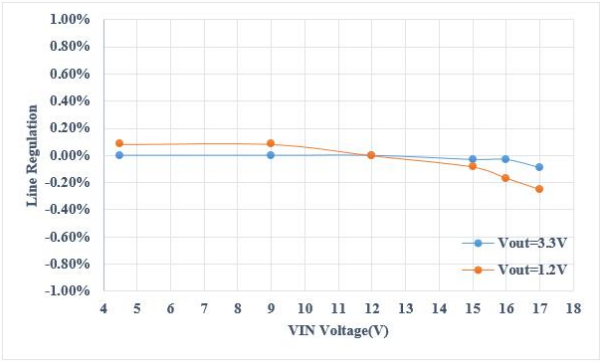


Figure 8. Line Regulation, I_{OUT} = 3A

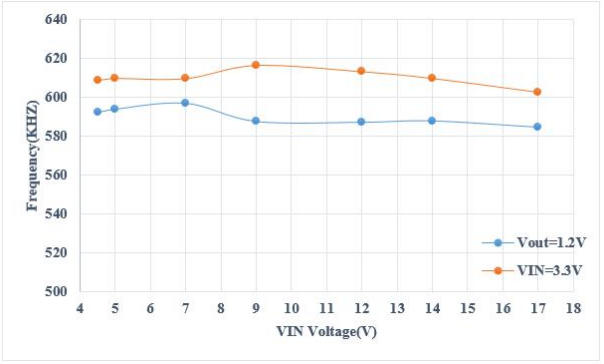


Figure 9. Switching Frequency vs. Input Voltage, I_{OUT} = 3A

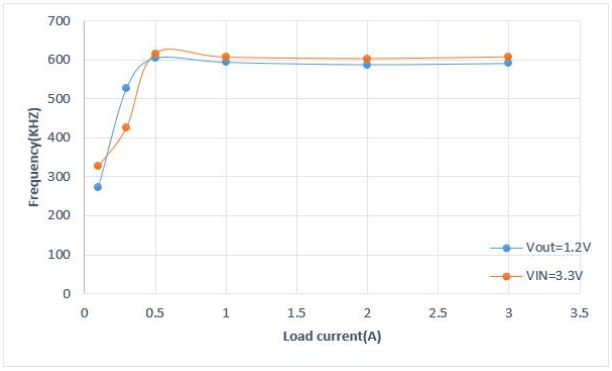


Figure 10. Switching Frequency vs. Load, V_{IN} = 12V

Typical Characteristics (Continued)

ΔV_{OUT}: 50mV/div; I_{OUT}: 1A/div

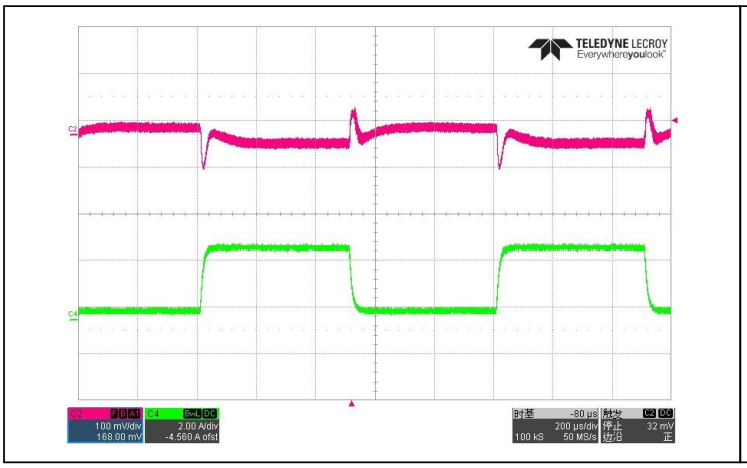


Figure 11. Load Transient
0.1 to 1.5A, 1A/μs slew rate

ΔV_{OUT}: 100mV/div; I_{OUT}: 2A/div

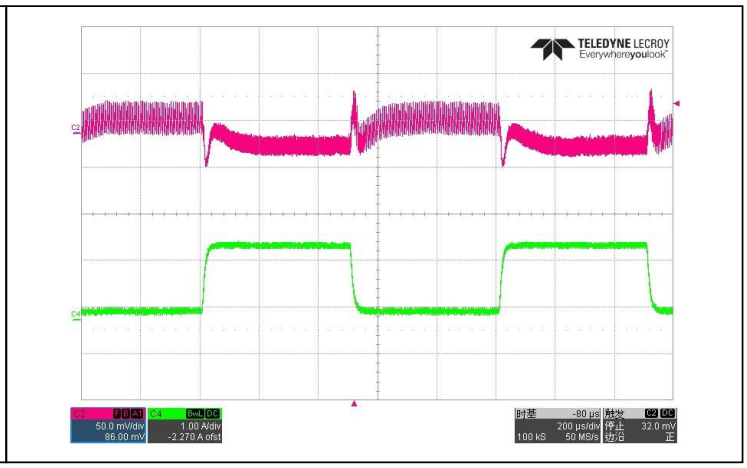


Figure 12. Load Transient
0.3 to 3A, 1A/μs slew rate

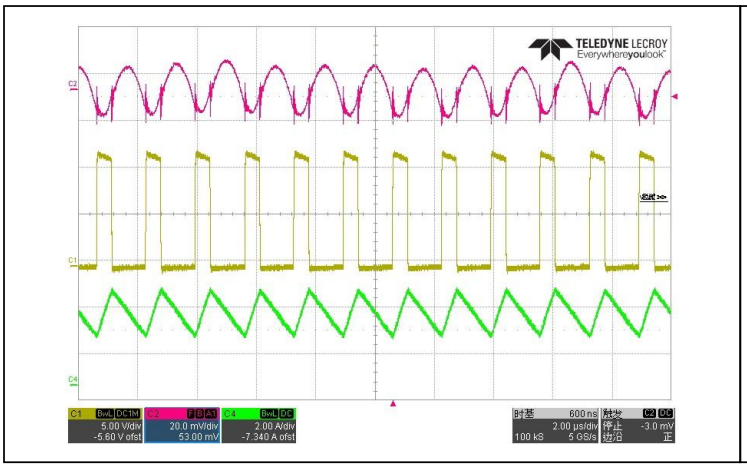


Figure 13. CCM Mode, I_{OUT} = 3A

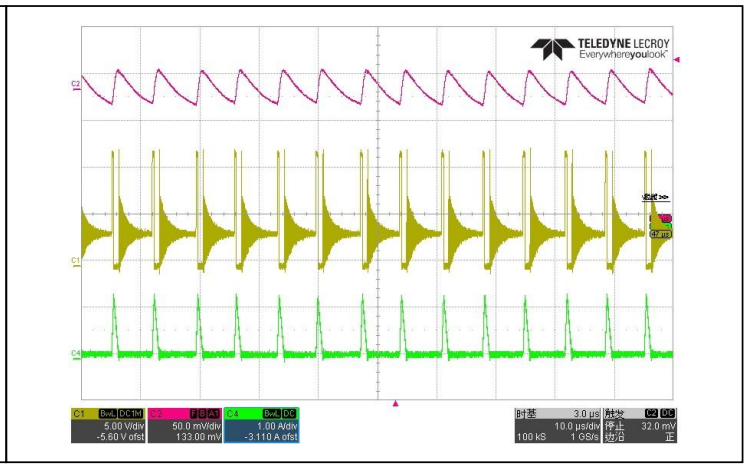


Figure 14. DCM Mode, I_{OUT} = 0.1A

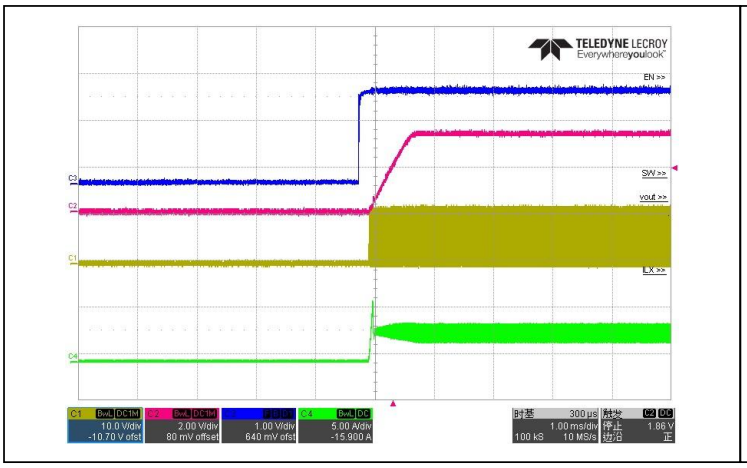


Figure 15. EN Startup with Load
I_{OUT} = 3A

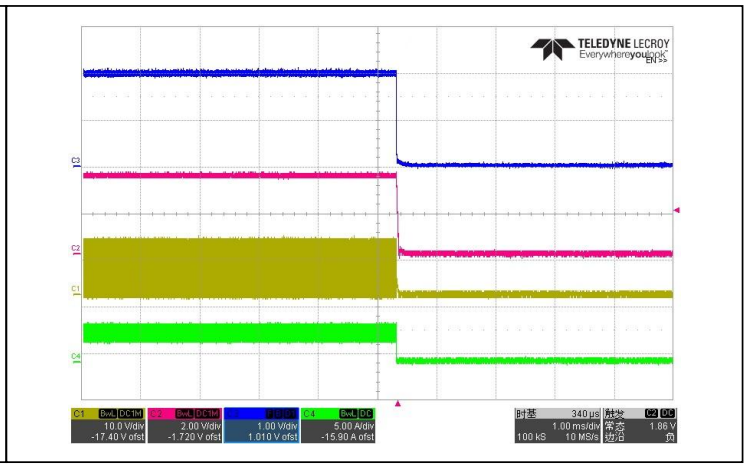


Figure 16. EN Shutdown with Load
I_{OUT} = 3A

Functions Description

Feature Description

The HCR3123D/HCR3123FD is a COT mode step-down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 1.5MHz operating frequency to ensure a compact, high efficiency design with excellent DC performance.

Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 160°C typically. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

Soft Start

The soft start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.8V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally max to 1500μs.

Startup and Shutdown

If both V_{IN} and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, V_{IN} low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The comp voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

Input Over-Voltage Protection (OVP)

The HCR3123D/HCR3123FD integrates input over-voltage protection. The OVP circuitry detects over-voltage condition by monitoring the input voltage. When input voltage rises above the OVP threshold, the OVP comparator turns high and both HS-FET and LS-FET are turned off. Once V_{IN} drops below OVP falling threshold, the IC starts switching again. This function can ensure the reliability when the input voltage is unstable with over-voltage spike.

Application Information

The output stage of a synchronous buck converter is mainly composed of inductor and capacitors. By switching the internally integrated power MOSFET, the energy is stored and transferred to the load, and the second-order LC filter is formed to smooth the switching node voltage so that the stable output DC voltage is obtained.

Setting Output Voltage

The output voltage is set by FB voltage, which is divided by resistor (R_1 and R_2) from output node to ground. A resistor with 1% or higher accuracy is preferred. The output voltage value is set by the equation below.

$$V_{OUT} = V_{FB} \times \frac{R_1 + R_2}{R_2}$$

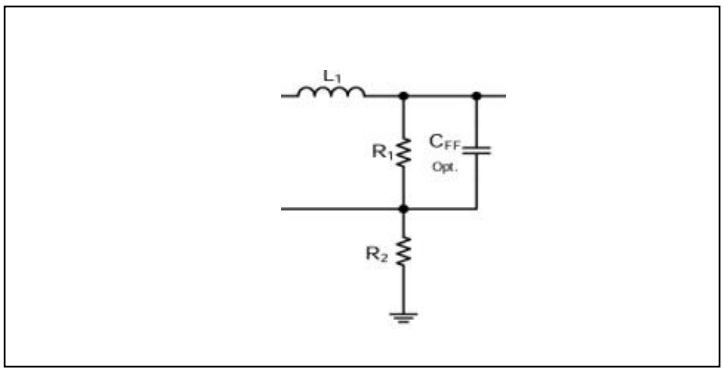


Figure 17. Setting Output Voltage

V_{REF} is the internal reference voltage of HCR3123D/HCR3123FD, 0.8V.

Table 1. Recommended Component Selection

V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)	BS (μF)	L_1 (μH)	C_{IN} (μF)	C_{OUT} (μF)	C_{FF} (pF) Optional
1.0	2.49	10	0.1	1R0 to 4R7	22	22 × 2	0 to 100
1.05	3.16	10	0.1	1R0 to 4R7	22	22 × 2	0 to 100
1.2	4.99	10	0.1	1R0 to 4R7	22	22 × 2	0 to 100
1.5	8.87	10	0.1	2R2 to 4R7	22	22 × 2	0 to 100
1.8	12.7	10	0.1	2R2 to 4R7	22	22 × 2	0 to 100
3.3	31.6	10	0.1	2R2 to 4R7	22	22 × 2	0 to 100
5.0	52.3	10	0.1	4R7	22	22 × 2	0 to 100

Application Information (Continued)

Inductor Selection

An inductor is required to supply constant current to the load while being driven by the switched input voltage. The common value of the inductance is between 1μH to 10μH. A larger value inductor will result in less current ripple and lower output voltage ripple. However, the larger value inductor will have larger physical size, higher DC resistance, and/or lower saturation current. A good rule to calculate the inductance is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum load current. At the same time, it is needed to make sure that the peak inductor current is below the inductor saturation current.

The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \times \Delta I_L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, fs is the switching frequency, and ΔL is the peak-to-peak inductor ripple current.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Input Capacitors Selection

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the converter. It is recommended to use low ESR capacitors to optimize the performance. A ceramic capacitor is preferred, but tantalum or low ESR electrolytic capacitors may also meet the requirements. It is better to choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C_{IN}) absorbs the input switching current, a good ripple current rating is required for the capacitor. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{load}\sqrt{\frac{V_{OUT}}{V_{IN}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, where:

$$I_{CIN} = \frac{I_{load}}{2}$$

For simplification, choose the input capacitor whose RMS current rating is greater than half of the maximum load current. When electrolytic or tantalum capacitors are used, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When ceramic capacitors are used, make sure that they have enough capacitance to maintain voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{load}}{f_s C_{IN}}\frac{V_{OUT}}{V_{IN}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

C_{IN} is the input capacitance.

Application Information (Continued)

Output Capacitors Selection

The output capacitor (C_{OUT}) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)\left(R_{ESR} + \frac{1}{8 f_s C_{OUT}}\right)$$

Where L is the inductor value, R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor and C_{OUT} is the output capacitance value. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly determined by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 f_s^2 L C_{OUT}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The HCR3123D/HCR3123FD can be optimized for a wide range of capacitance and ESR values.

Feed-Forward Capacitor Selection (C_{FF})

HCR3123D/HCR3123FD has internal loop compensation, so adding C_{FF} is optional. Specifically, consider whether to add feed-forward capacitors according to the situation.

The use of a feed-forward capacitor (C_{FF}) in the feedback network is to improve the transient response or higher phase margin. To reduce transient ripple, the feed-forward capacitor value can be increased to push the cross frequency to a higher region. Although this can improve transient response, it also decreases phase margin and causes more ringing. On the other hand, if more phase margin is desired, the feed-forward capacitor value can be decreased to push the cross frequency to a lower region.

The value of feed-forward capacitor (C_{FF}) can be calculated with the following equation:

$$C_{ff_op} = \frac{1}{2\pi f_{nocff}}\sqrt{\frac{1}{R_1}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)}$$

Where F_nocff is the cross frequency. The crossing frequency is generally taken as 1/10 to 1/5 of the switching frequency, R_1 and R_2 are feedback resistors.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between the VBST to SW pin for proper operation. A ceramic capacitor is recommended.

PCB Layout

PCB layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion efficiency, thermal performance, and minimized EMI.

1. The feedback network, resistor R_1 and R_2, should be kept close to the FB pin. The V_{OUT} sense path should stay away from noisy nodes, such as SW and BS signals, and preferably through a layer on the other side of the shielding layer.

2. The input bypass capacitors C_5 and C_2 must be placed as close as possible to the V_{IN} pin and ground. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the GND pin and PAD. It is a good practice to place a ceramic cap near the V_{IN} pin to reduce the high frequency injection current.

3. The inductor L should be placed close to the SW pin to reduce magnetic and electrostatic noise.

4. The output capacitor C_{OUT} should be placed close to the junction of L_1. The L_1 and C_{OUT} trace should be as short as possible to reduce conducted and radiated noise and increase overall efficiency.

5. The ground connection for C_5, C_2 and C_8, C_4, C_3 should be as small as possible and connect to the system ground plane at only one spot (preferably at the C_{OUT} ground point) to minimize injecting noise into the system ground plane.

6. Large GND copper pour near the IC is recommended to minimize the heat of the IC.

Layout Example

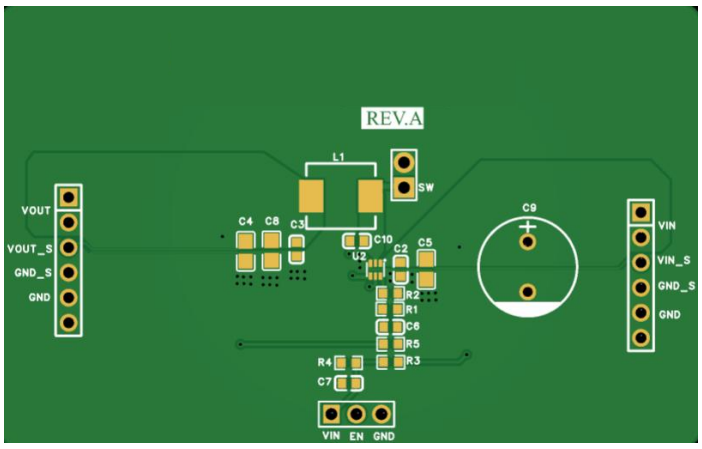


Figure 18. PCB Layout, Top Side

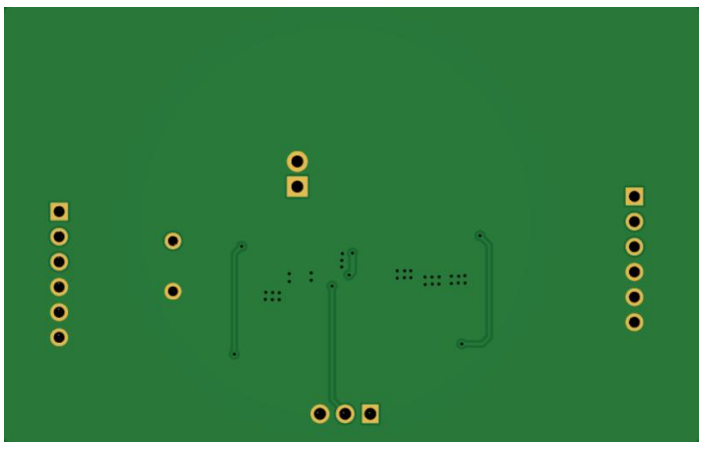


Figure 19. PCB Layout, Bottom Side

Package Outline Dimensions

PDFN-1.6×1.6-6L

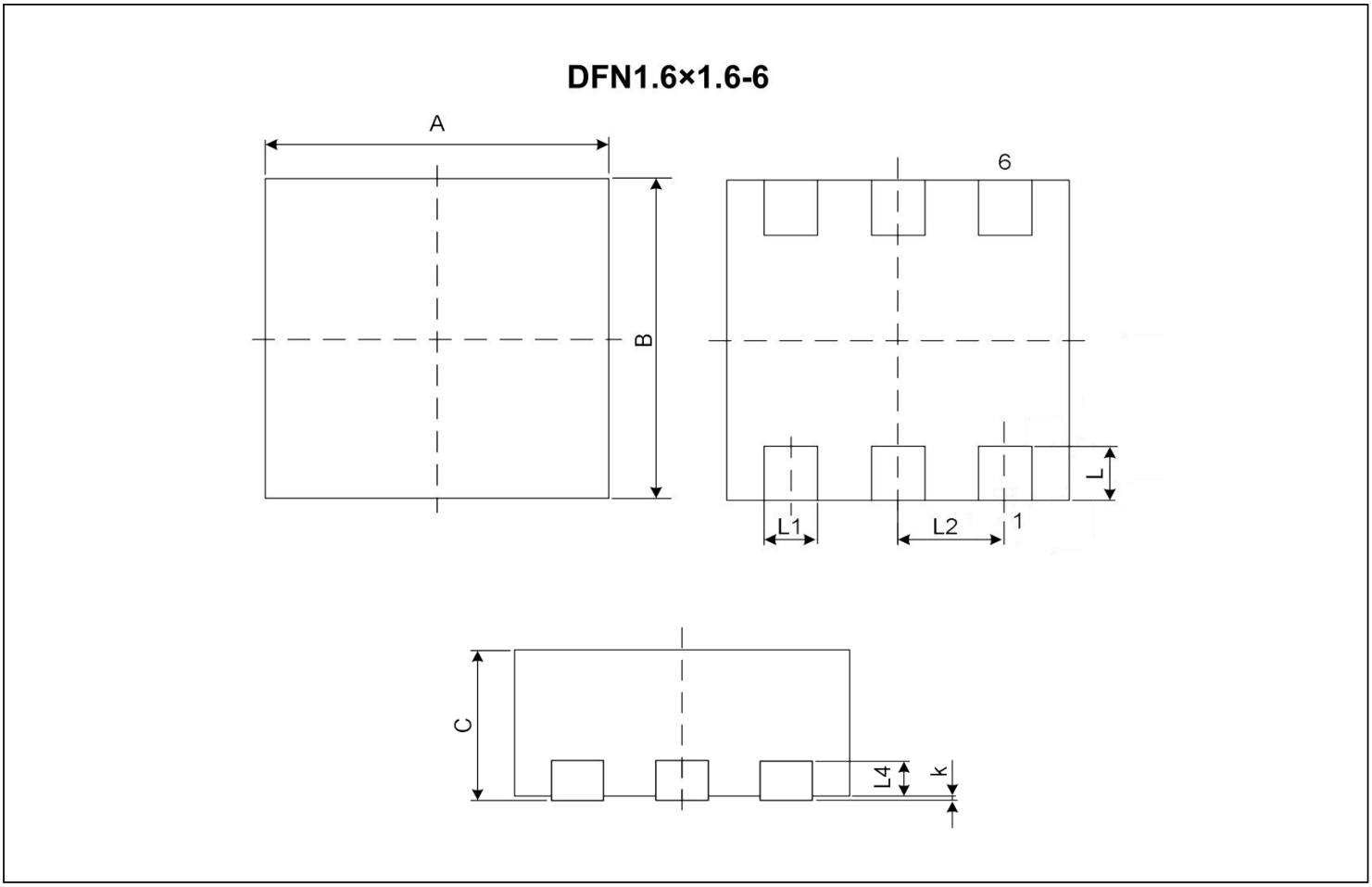


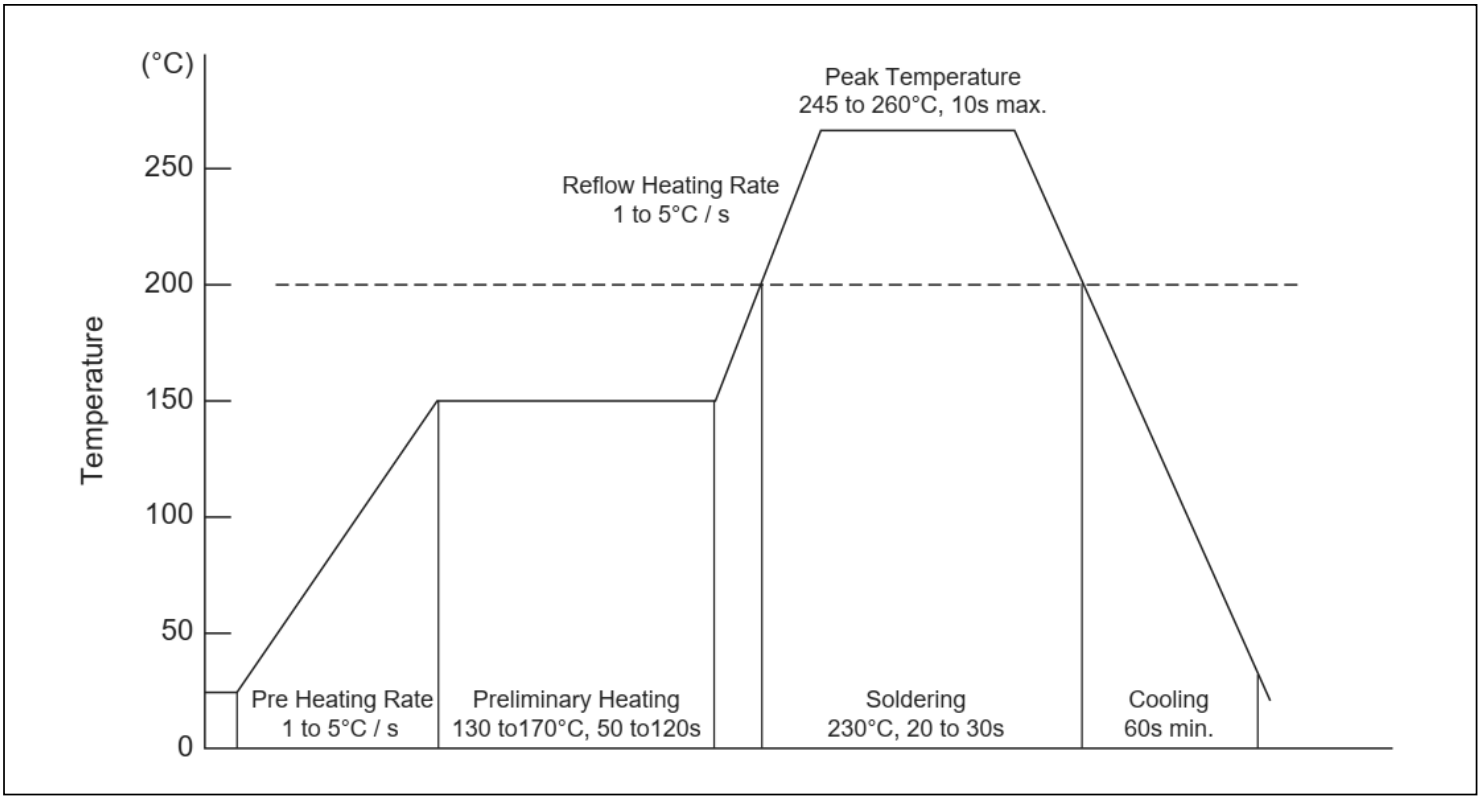
Figure 20. Package Outline Dimensions

Dimensions in Millimeters

Symbol	Min.	Typ.	Max.
A	1.500	1.600	1.650
B	1.500	1.600	1.650
C	0.700	0.750	0.800
L	0.230	0.275	0.330
L_1	0.200	0.250	0.300
L_2	-	0.500	-
L_4	-	0.203	-
k	0.000	0.020	0.050

Conditions of Soldering and Storage

Recommended condition of reflow soldering



Recommended peak temperature is over 245°C. If peak temperature is below 245°C, you may adjust the following parameters:

- Time length of peak temperature (longer)
- Time length of soldering (longer)
- Thickness of solder paste (thicker)

Conditions of Hand Soldering

- Temperature: 300°C
- Time: 3s max
- Times: one time

Storage Conditions

- Temperature: 5 to 40°C
- Humidity: 30 to 80% RH
- Recommended period: one year after manufacturing